

PGRAA

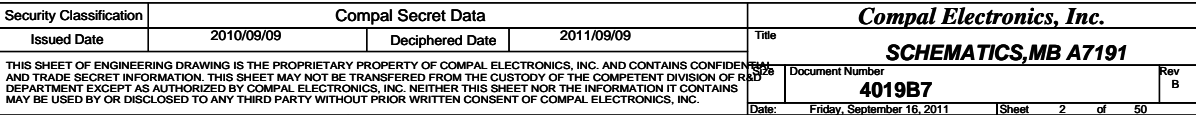
Superior 10RH

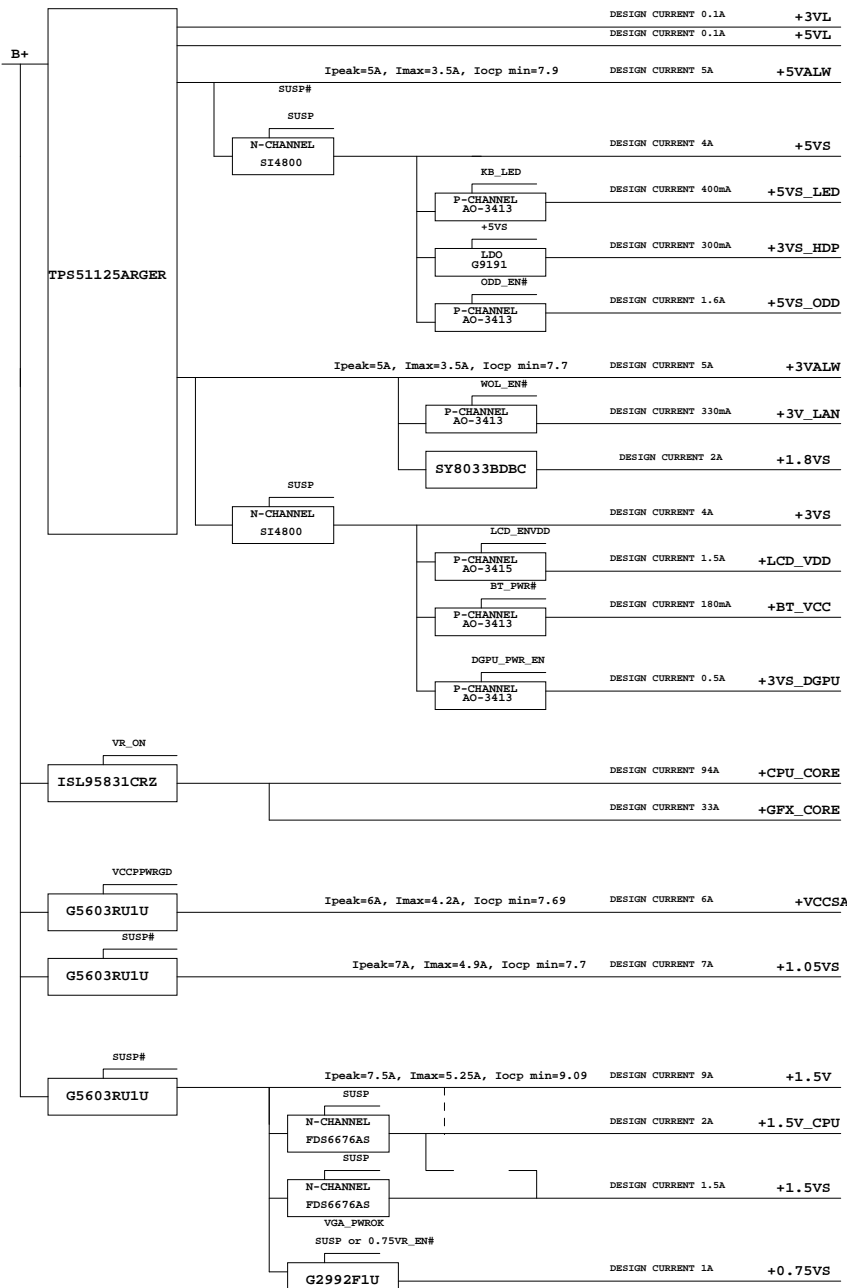
LA-7191P REV 1.0 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2011-04-26 Rev 1.0

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Model Name : PGRAA
File Name : LA-7191P





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				Rev	8

Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE +VTT +3VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

BTO Option Table

Platform	SKU	CPU	PCH
Huron River	Discrete (DIS@)	Clarksfield/ Arrandale	HM65
	Optimus (OPT@)	Arrandale	HM65

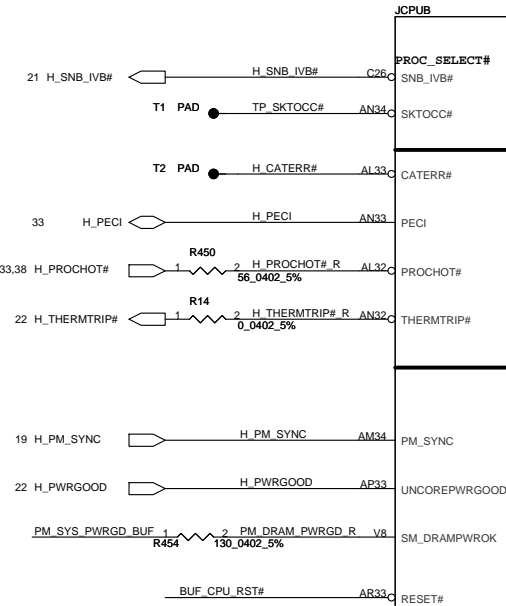
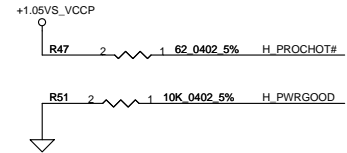
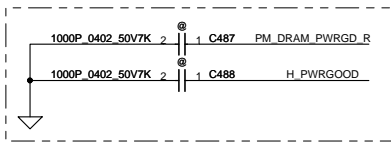
Function	HDMI		
description	HDMI		
explain	Optimus	Discrete	CEC
BTO	IHDMI@	DHDMI@	CEC@

Function	MINI PCI-E SLOT		Fingerprint	KB Light
description	SLOT2	SLOT1	Fingerprint	KB Light
explain		WIMAX	Fingerprint	KB Light
BTO			FP@	KBL@

Function	BLUE TOOTH	SKU		LVDS		CIR
description	BLUE TOOTH	SKU		3D Panel		CIR
explain	BLUE TOOTH	Discrete	Optimus	Discrete	Optimus	CIR
BTO	BT@	DIS@	OPT@	DIS@	OPT@	CIR@

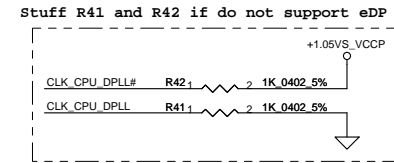
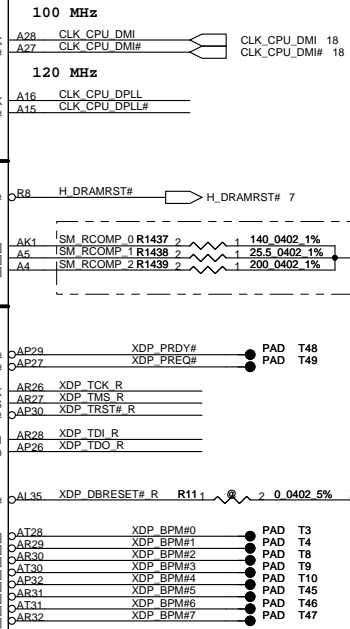
Function	EC			
description				
explain	KB930QF	KB9012QF	Trial run phase	MP Phase
BTO	930@	9012@	DBG@	MP@

<div>STATE</div> <div>SIGNAL</div>	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

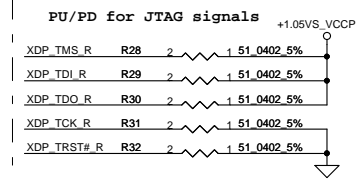
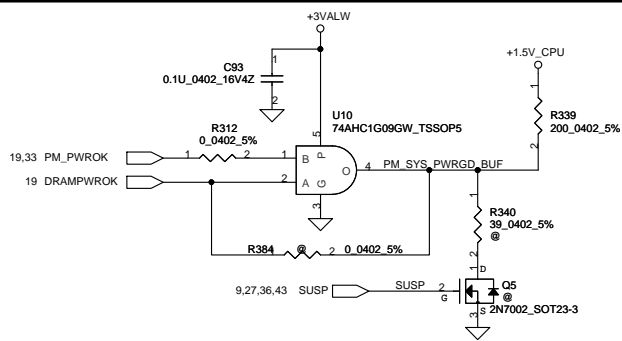
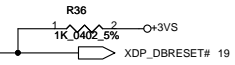


JCPU
PROC_SELECT#
SNB_IVB#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWGOOD
SM_DRAMPWROK
RESET#
Sandy Bridge_rPGA_Rev0p61

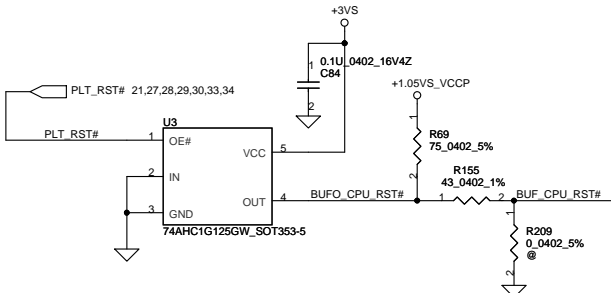
MISC
CLOCKS
DDR3 MISC
JTAG & BPM
BCLK
BCLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]



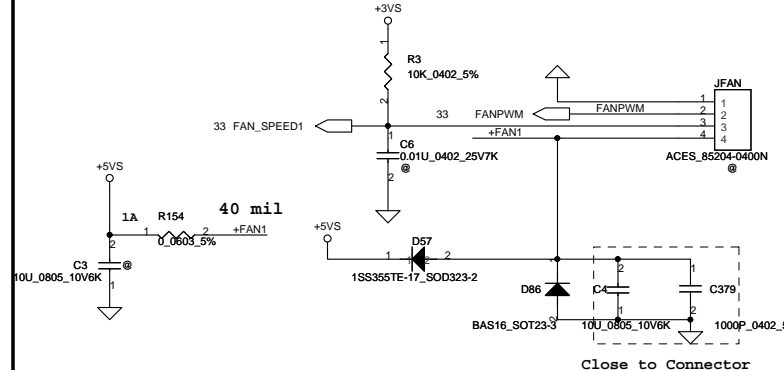
DDR3 Compensation Signals
Layout Note: Place these resistors near Processor



Buffered Reset to CPU

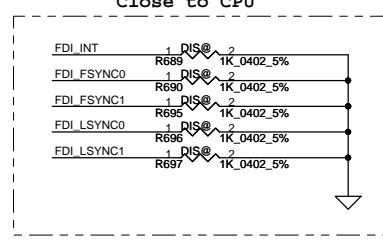
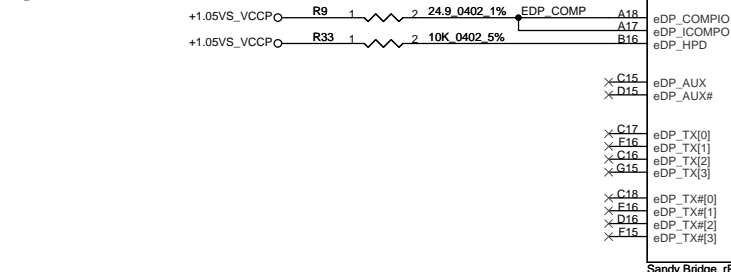


FAN Control Circuit



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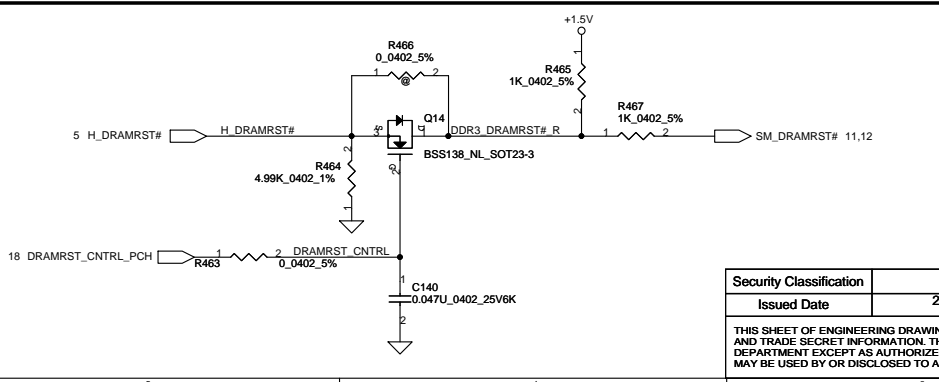
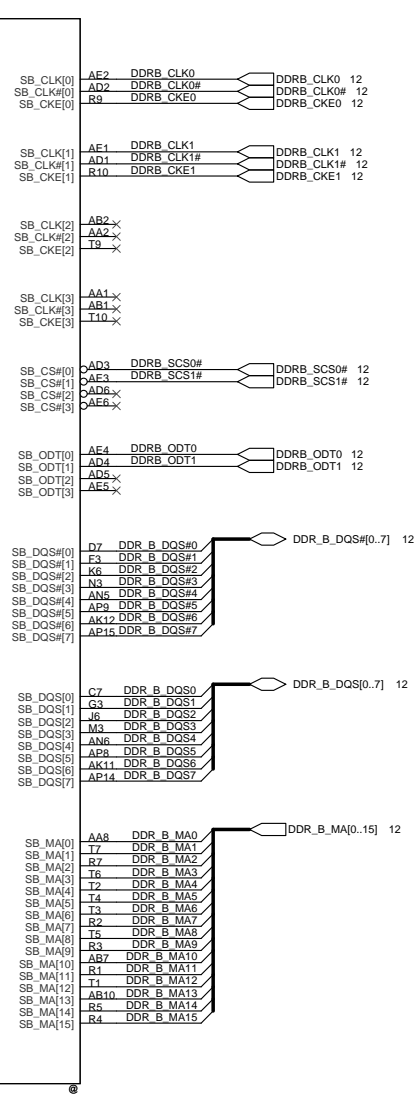
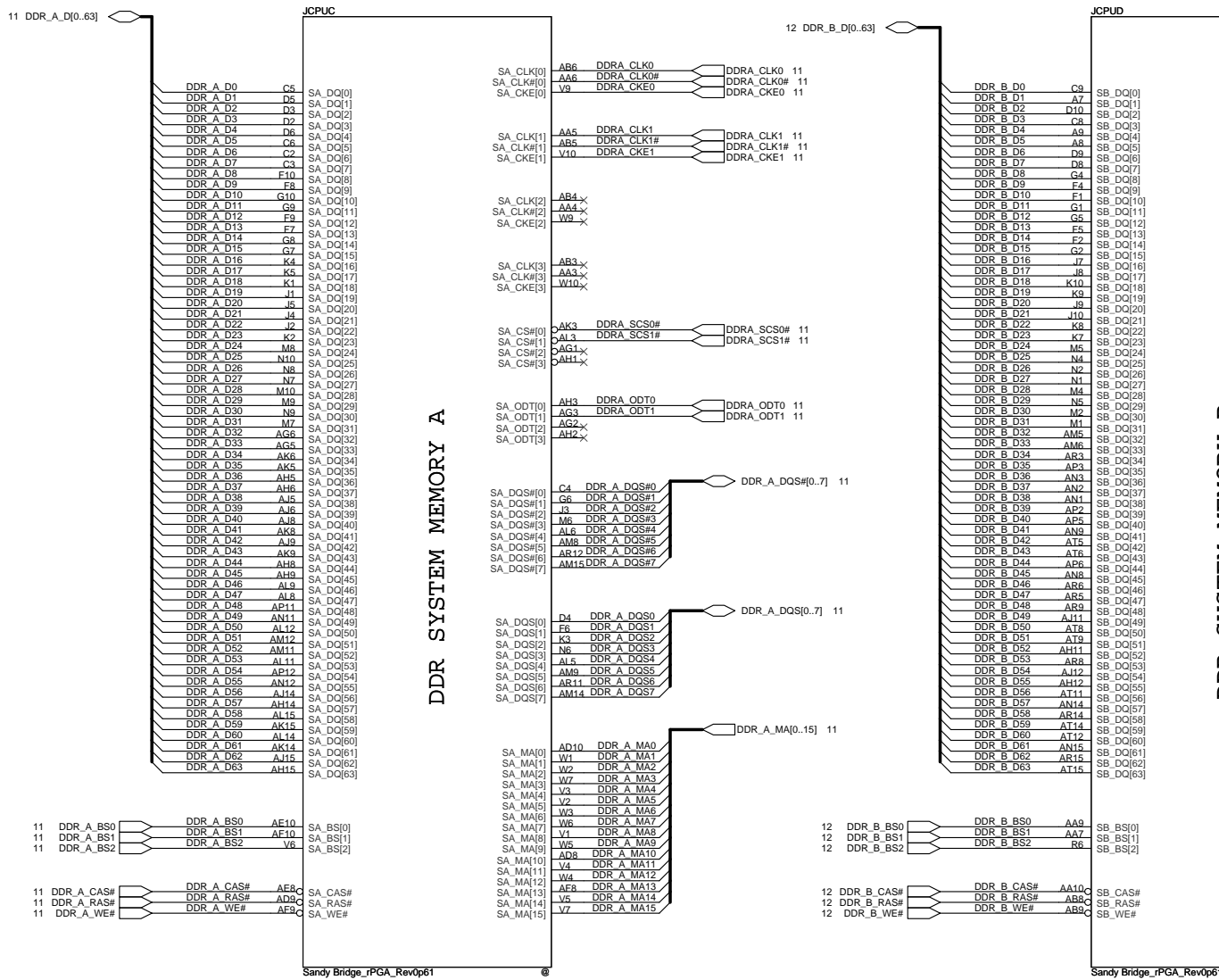
eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm



Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

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CORE SUPPLY

PEG AND DDR

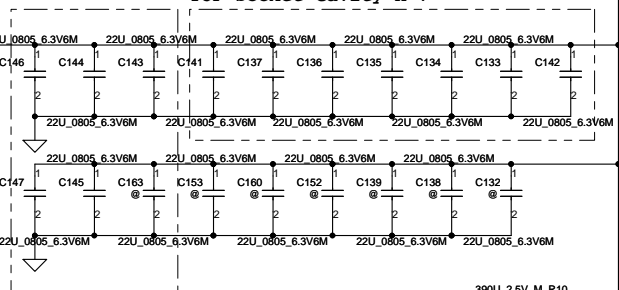
SVIID

SENSE LINES

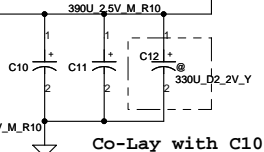
8.5A

+1.05VS_VCCP

TOP Socket Cavity x 7



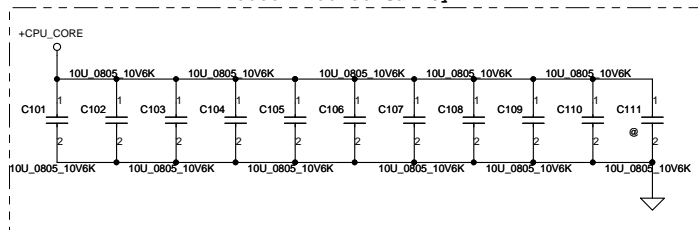
Bottom Socket Cavity x 5



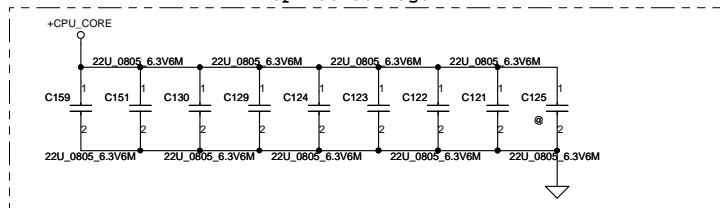
Co-Lay with C10

```
+CPU_CORE Decoupling:
4X 330U (6m ohm), 16X 22U, 10X 10U
```

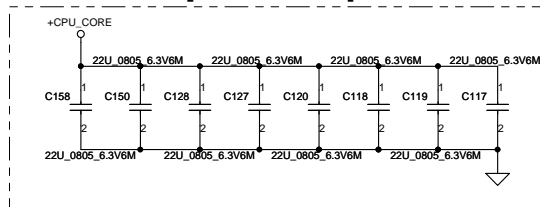
Bottom Socket Cavity



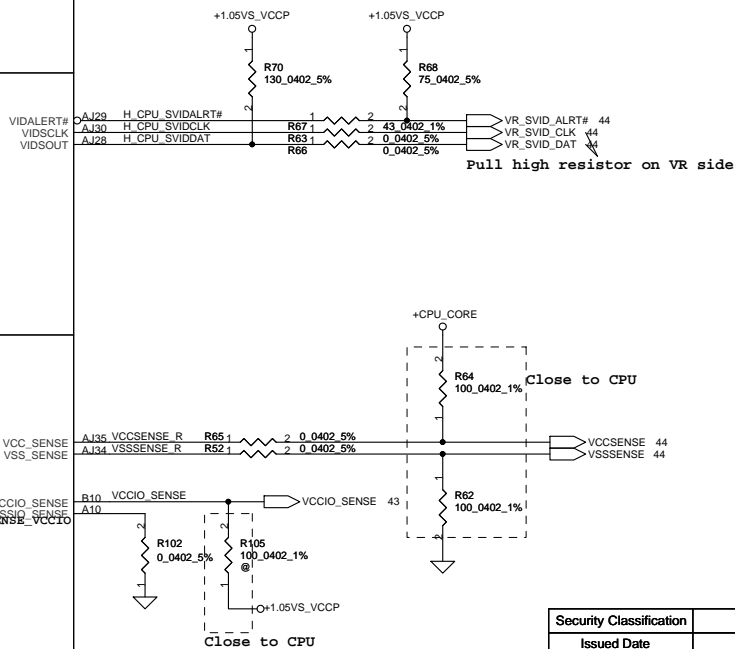
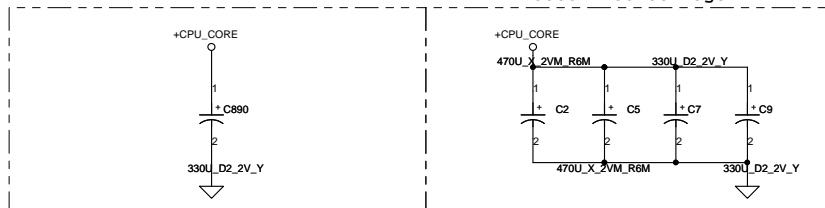
Top Socket Edge



Top Socket Cavity

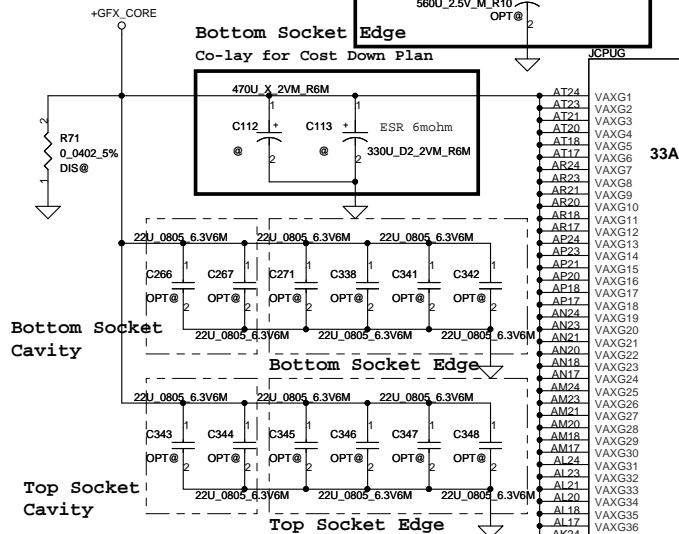


Bottom Socket Edge

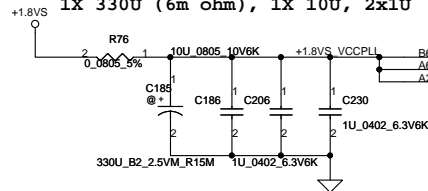


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+GFX_CORE Decoupling:
2X 330U (6m ohm), 12X 22U



VCCPLL Decoupling:
1X 330U (6m ohm), 1X 10U, 2x1U



1.2A
Sandy Bridge_PGA_RevOp61

GRAPHICS

1.8V RAIL

POWER

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

5A

6A

VCCSA_SENSE

VCCSA_VID0

FC_C22

VCCSA_VID1

VAXG1

VAXG2

VAXG3

VAXG4

VAXG5

VAXG6

VAXG7

VAXG8

VAXG9

VAXG10

VAXG11

VAXG12

VAXG13

VAXG14

VAXG15

VAXG16

VAXG17

VAXG18

VAXG19

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VAXG285

VAXG286

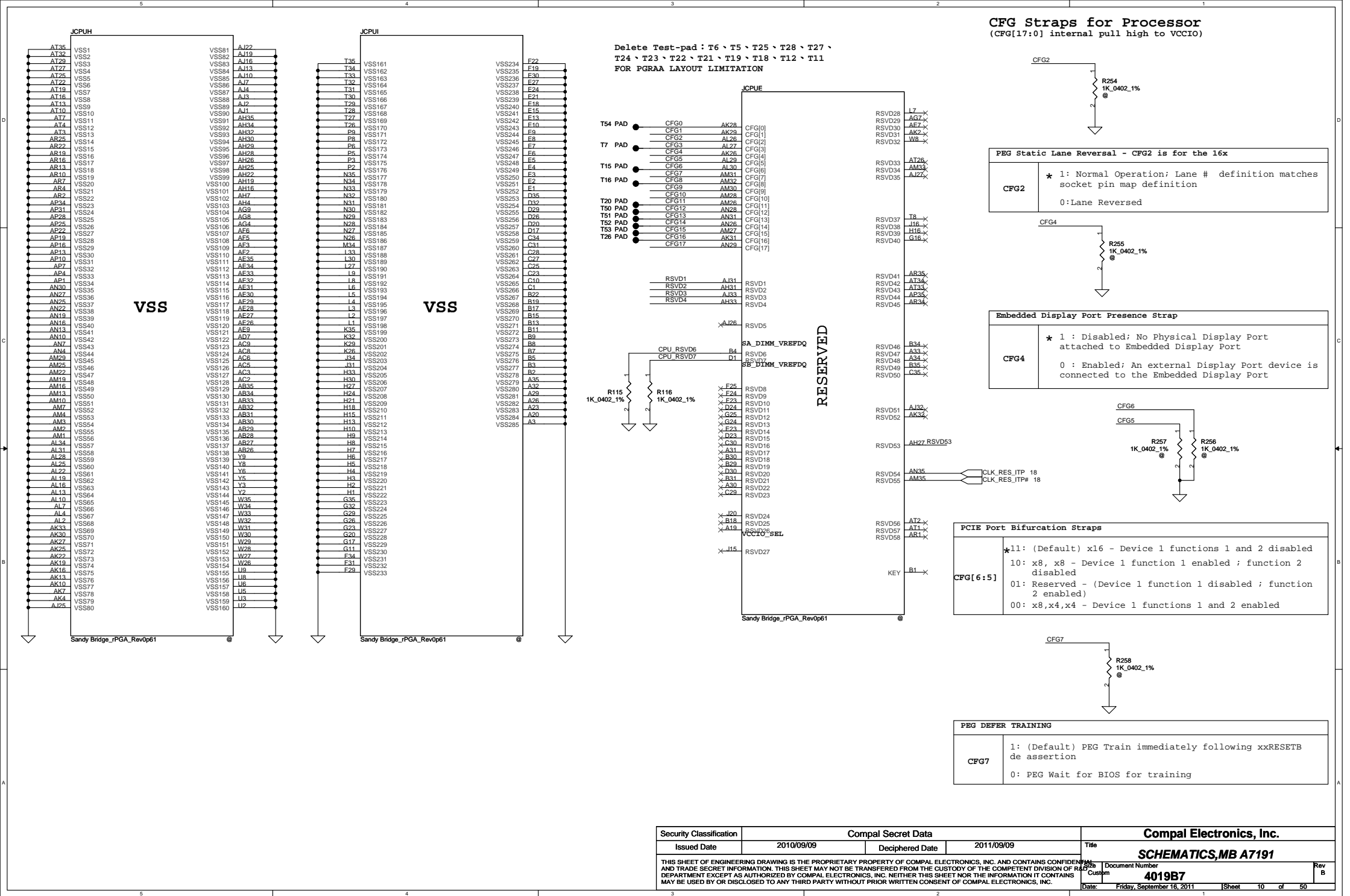
VAXG287

VAXG288

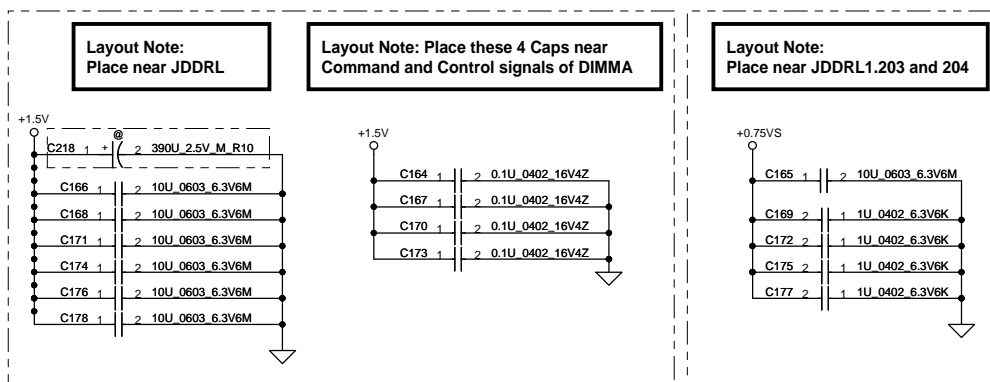
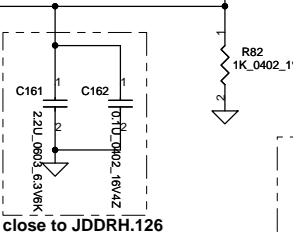
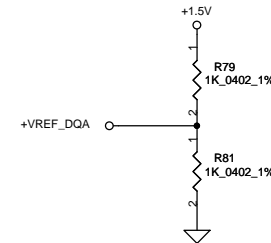
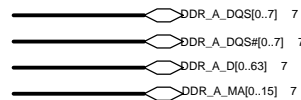
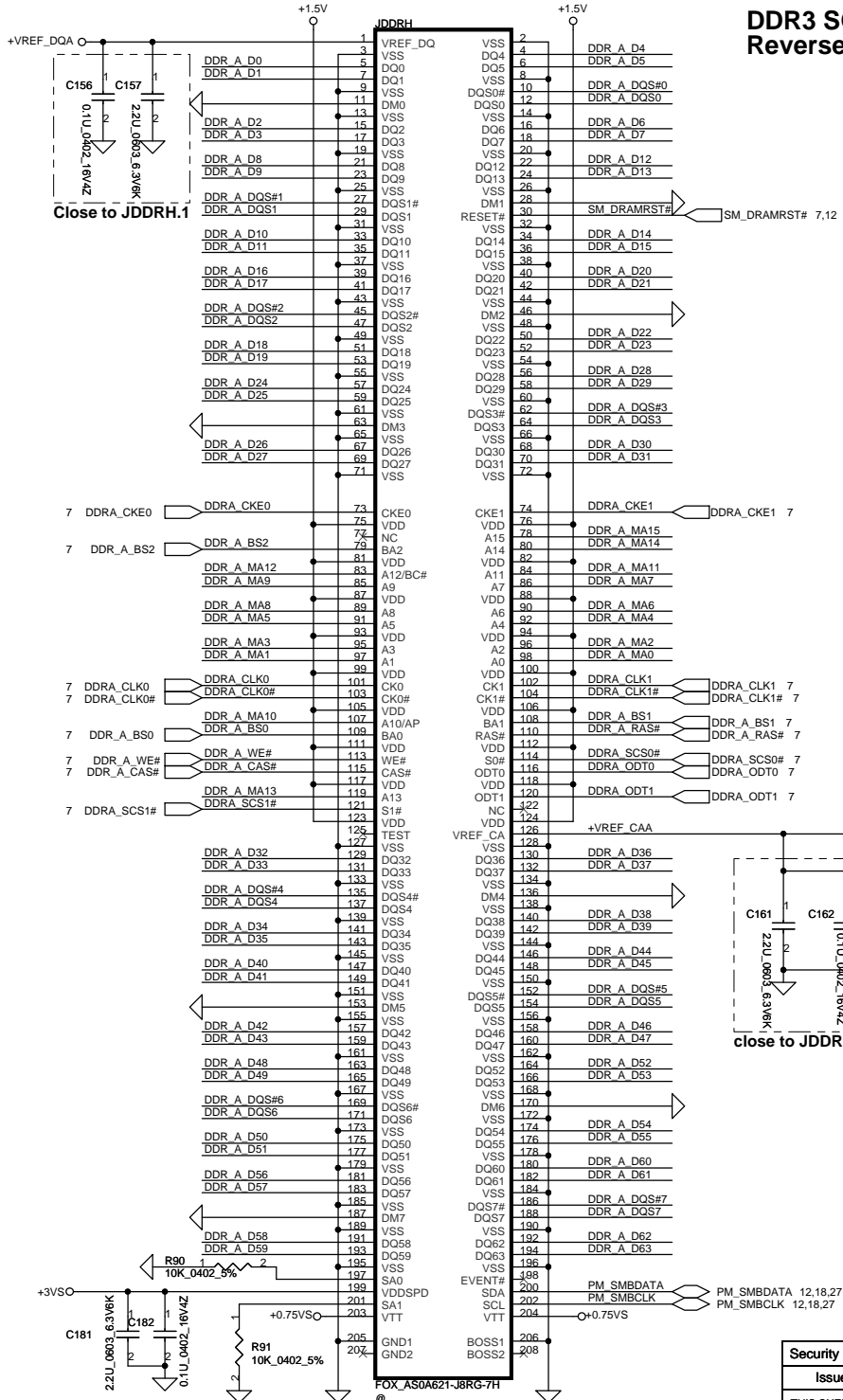
VAXG289

VAXG290

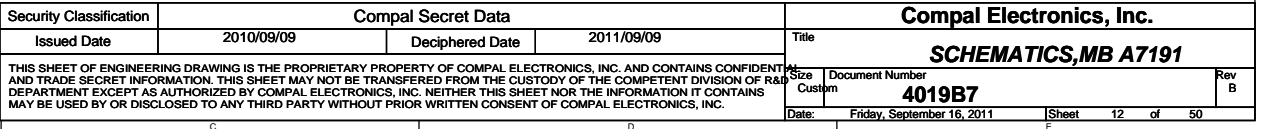
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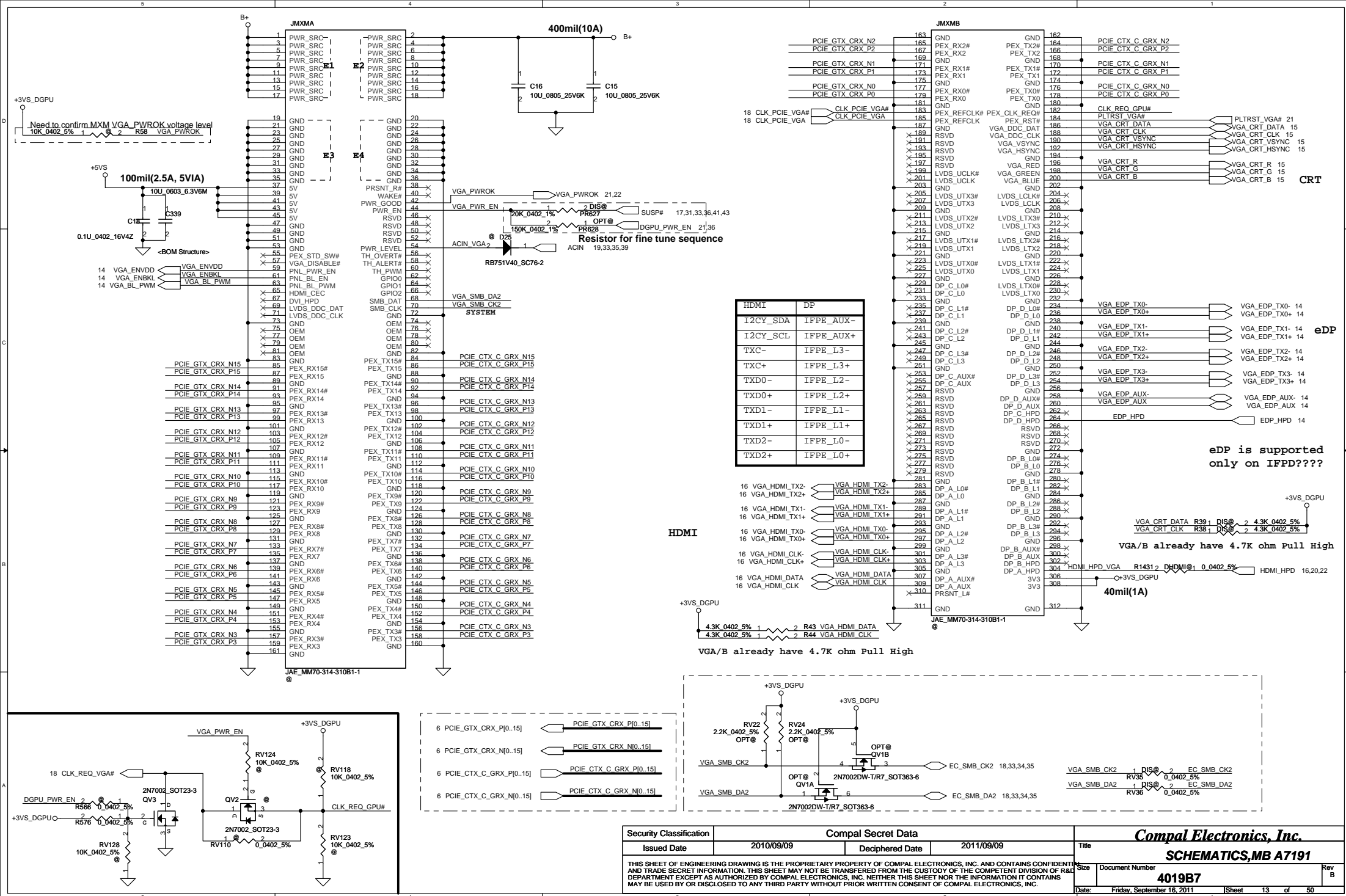


DDR3 SO-DIMM A Reverse Type

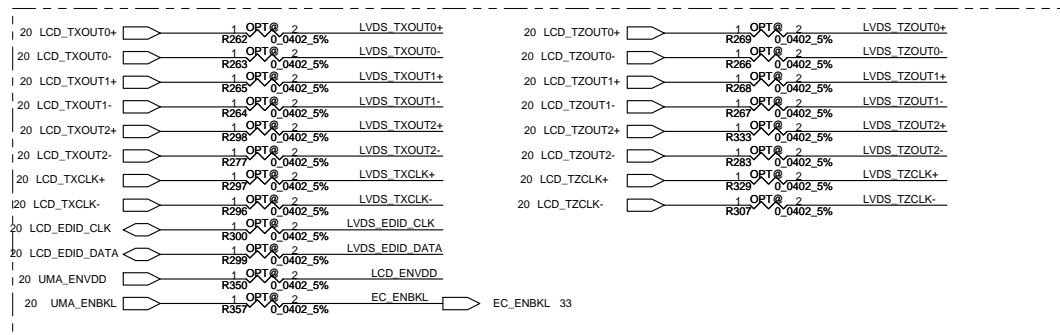


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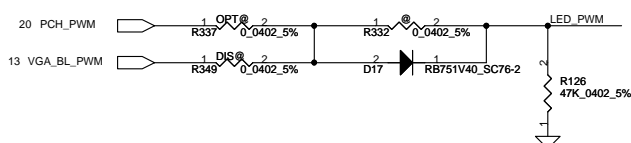




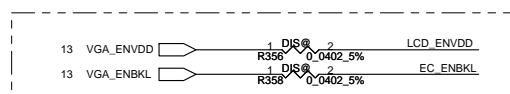
OPTIMUS



Close to LVDS Connector

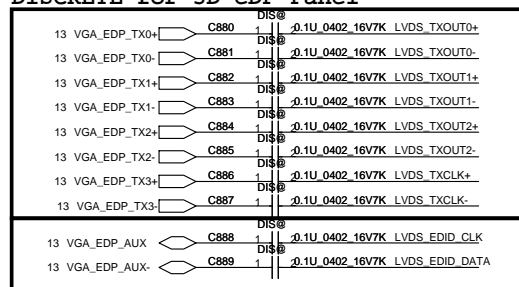


DISCRETE

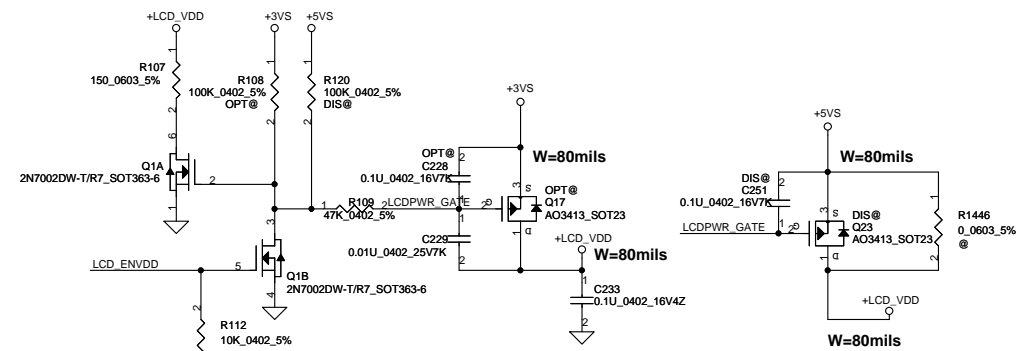


Close to LVDS Connector

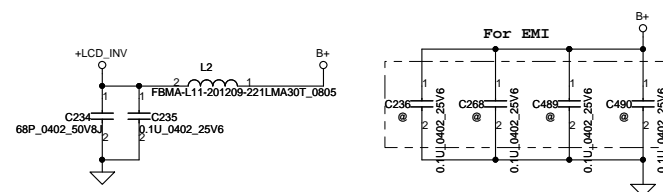
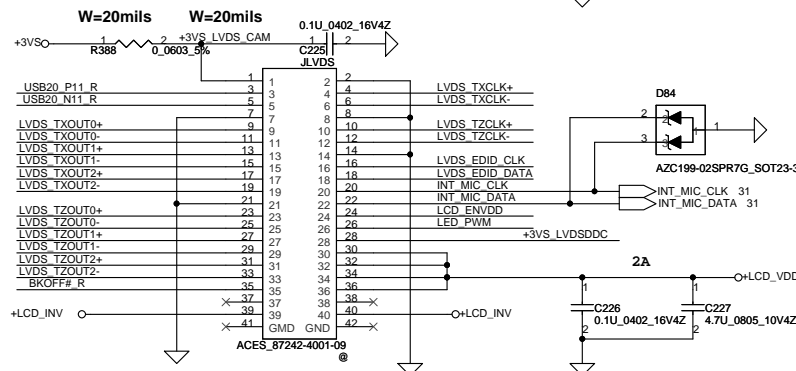
DISCRETE for 3D eDP Panel



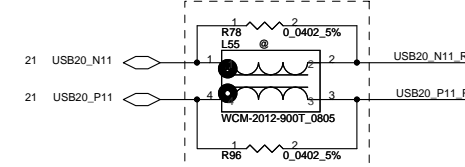
Close to LVDS Connector



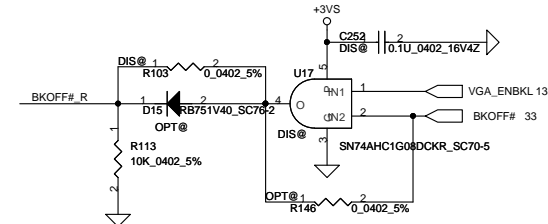
LCD/PANEL BD. Conn.



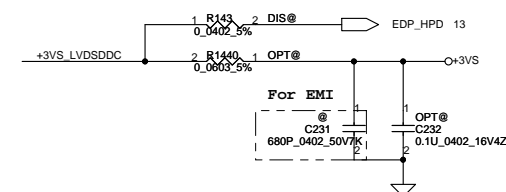
Reserve for EMI request



Reserve for eDP panel



Reserve for LVDS panel



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OPTIMUS

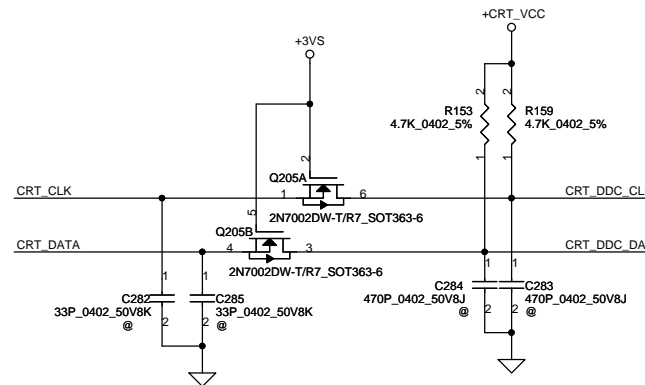
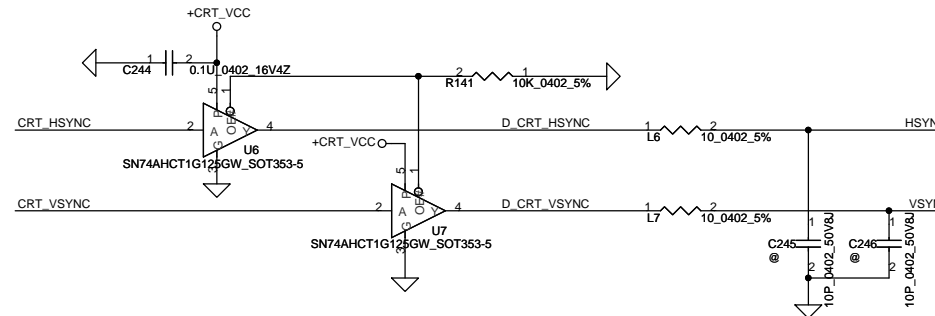
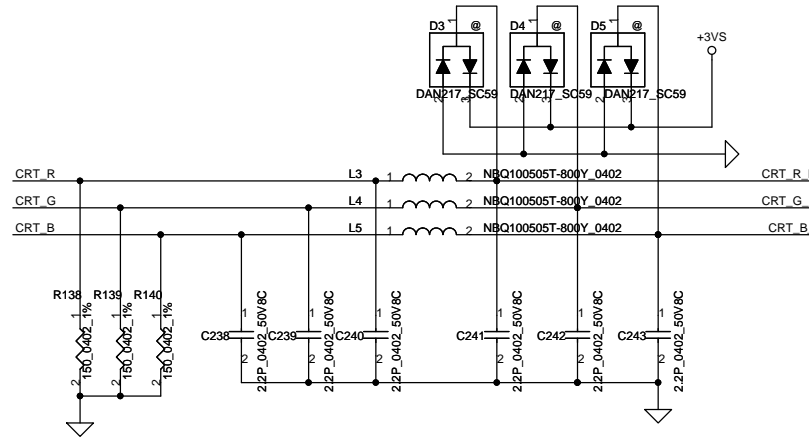
20	UMA_CRT_R	1	OPT	2	CRT_R
20	UMA_CRT_G	1	OPT	2	CRT_G
20	UMA_CRT_B	1	OPT	2	CRT_B
20	UMA_CRT_HSYNC	1	OPT	2	CRT_HSYNC
20	UMA_CRT_VSYNC	1	OPT	2	CRT_VSYNC
20	UMA_CRT_CLK	1	OPT	2	CRT_CLK
20	UMA_CRT_DATA	1	OPT	2	CRT_DATA

Close to CRT Connector

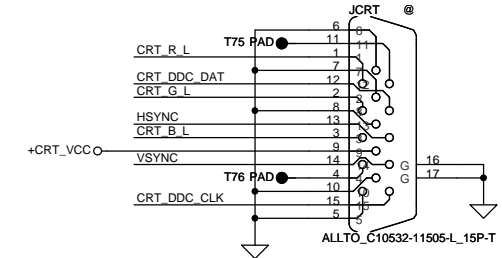
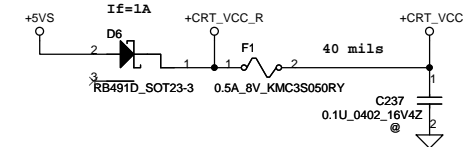
DISCRETE

13	VGA_CRT_R	1	DIS	2	CRT_R
13	VGA_CRT_G	1	DIS	2	CRT_G
13	VGA_CRT_B	1	DIS	2	CRT_B
13	VGA_CRT_HSYNC	1	DIS	2	CRT_HSYNC
13	VGA_CRT_VSYNC	1	DIS	2	CRT_VSYNC
13	VGA_CRT_CLK	1	DIS	2	CRT_CLK
13	VGA_CRT_DATA	1	DIS	2	CRT_DATA

Close to CRT Connector

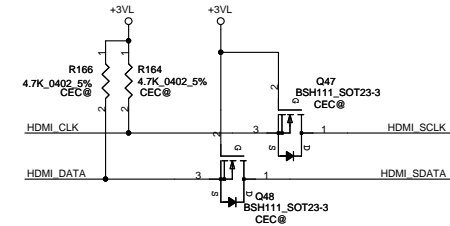
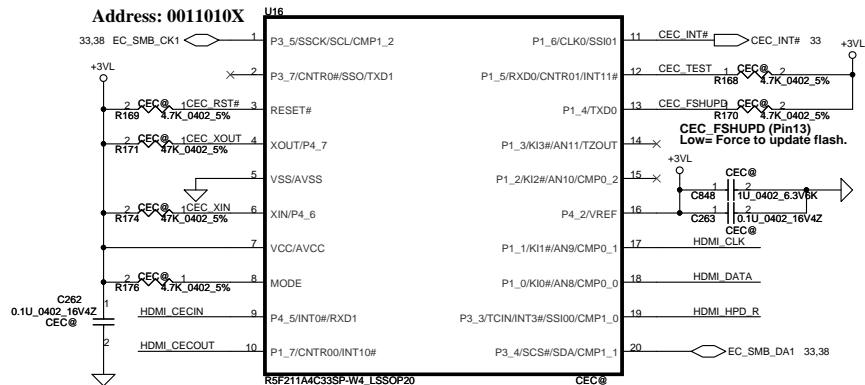
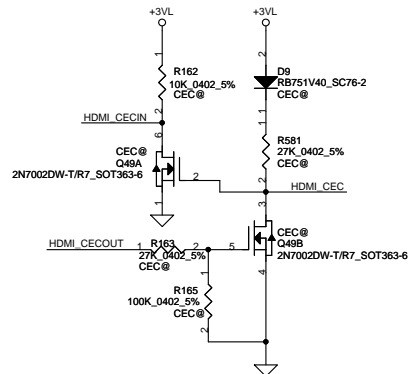


CRT CONNECTOR

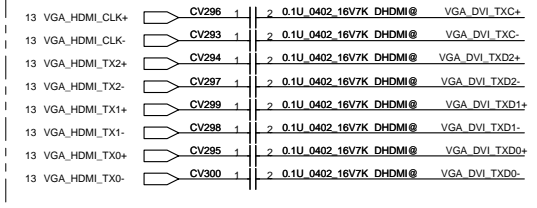


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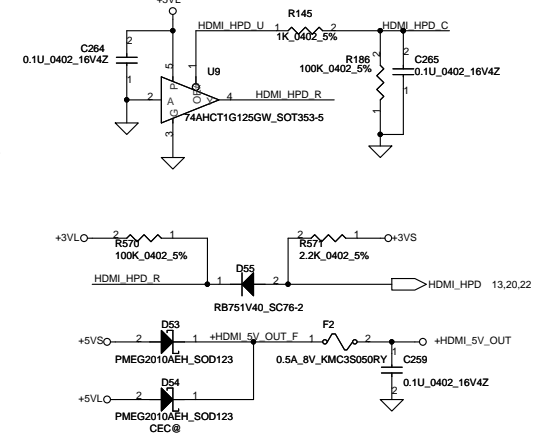
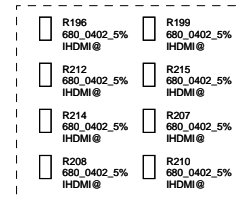
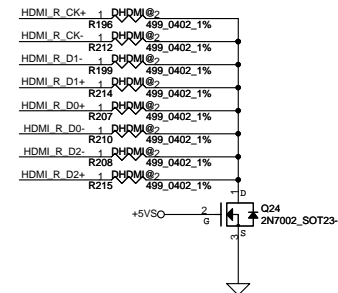
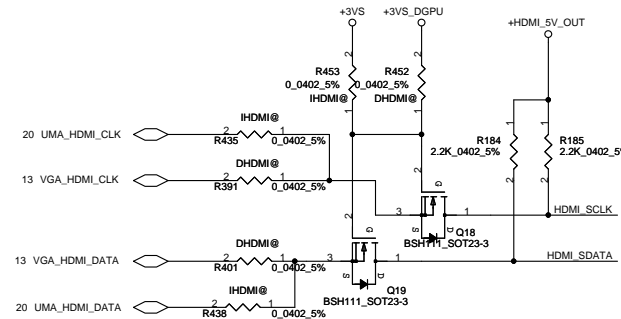
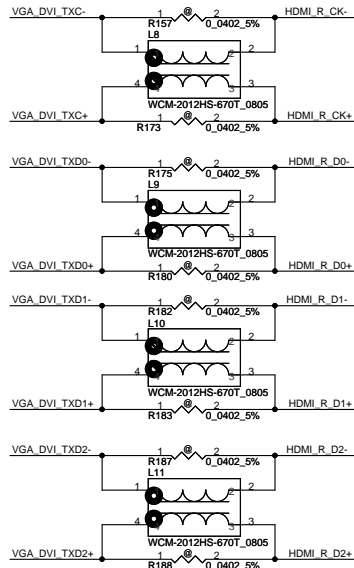
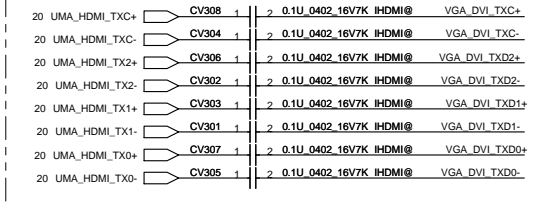
HDMI CEC Controller



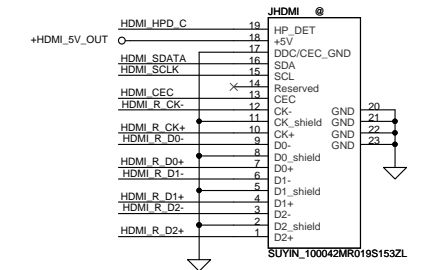
For DISCRETE



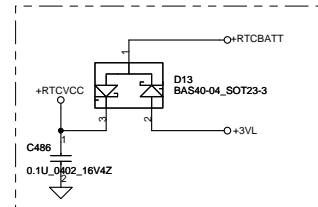
For Optimus

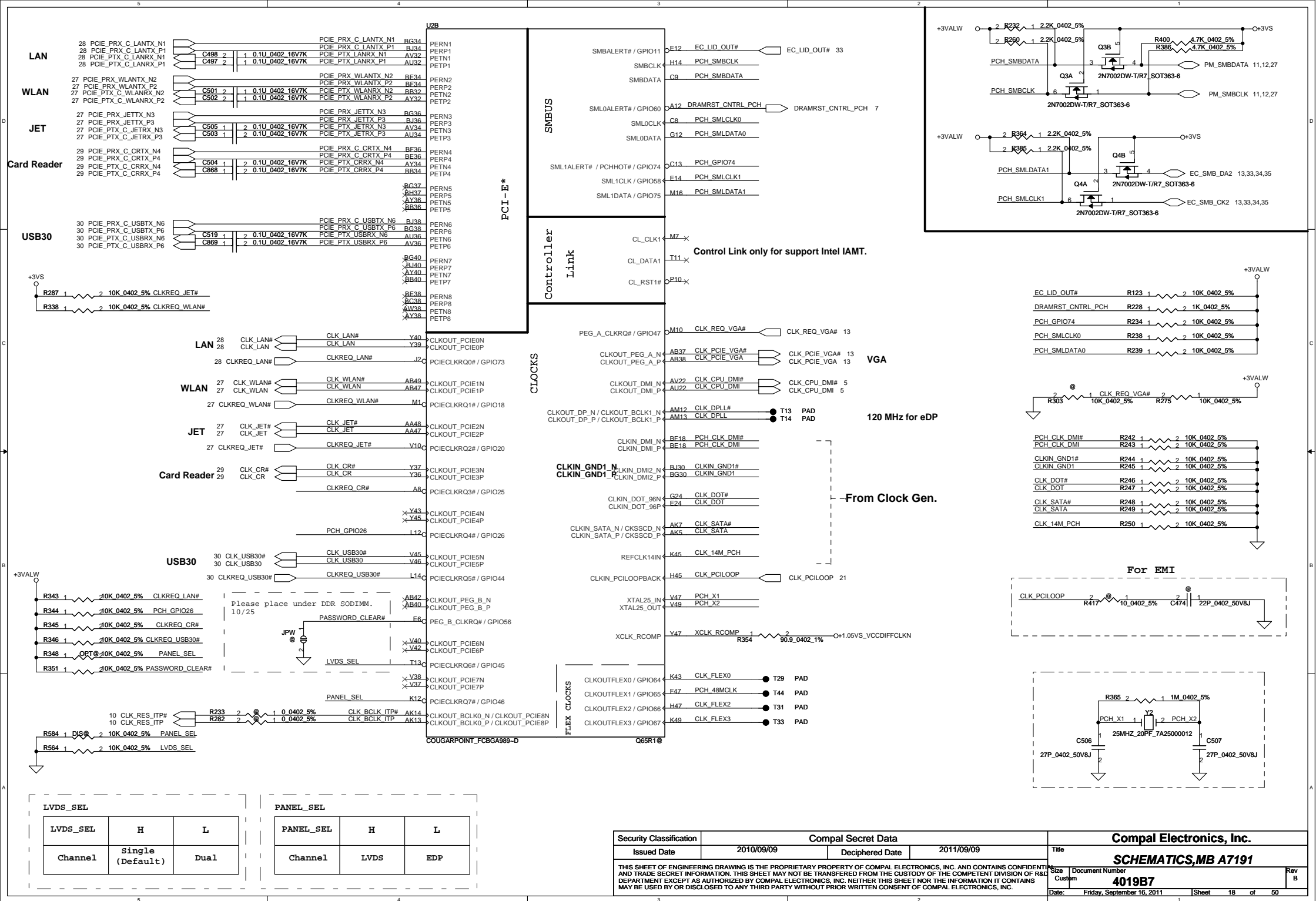


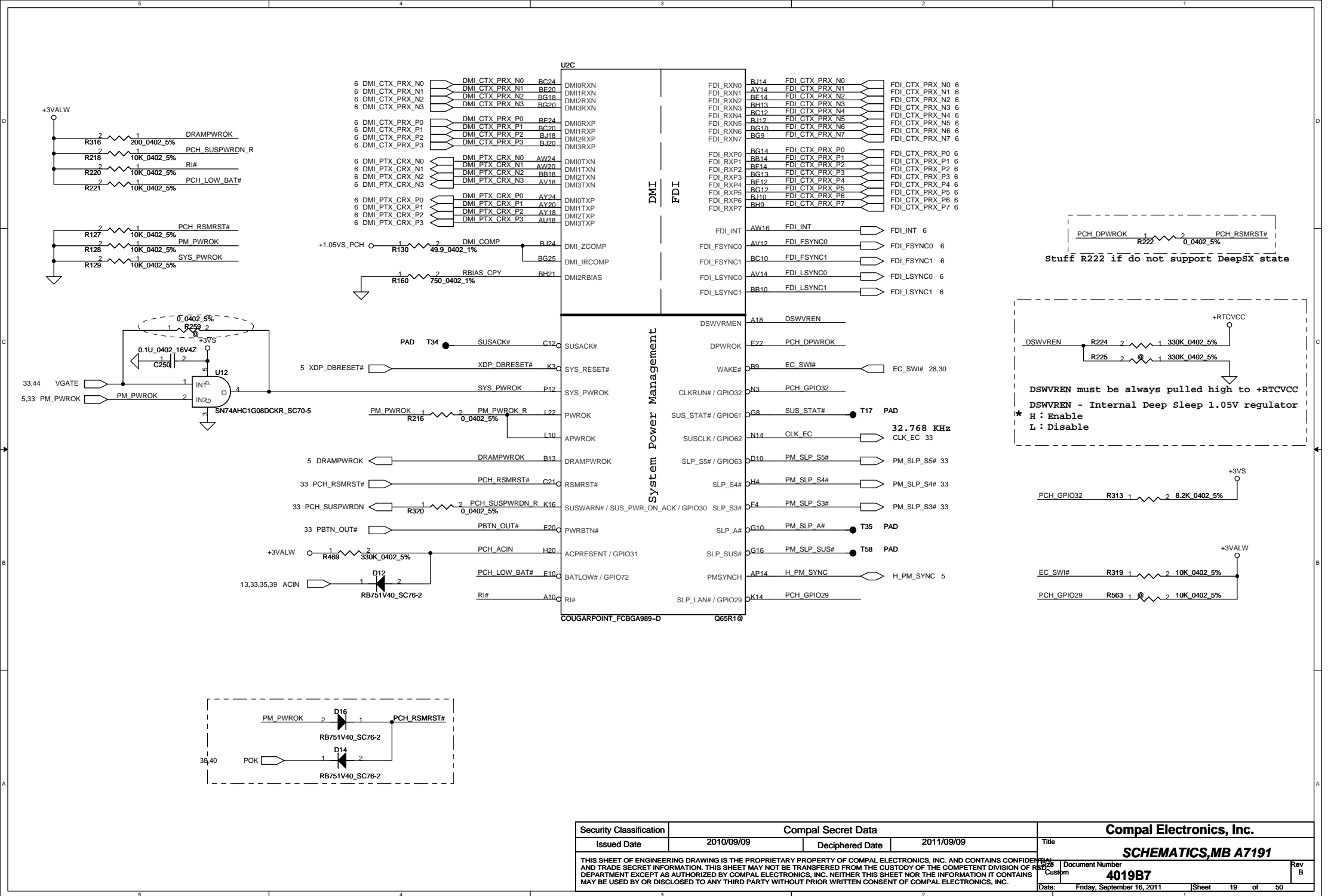
HDMI Connector

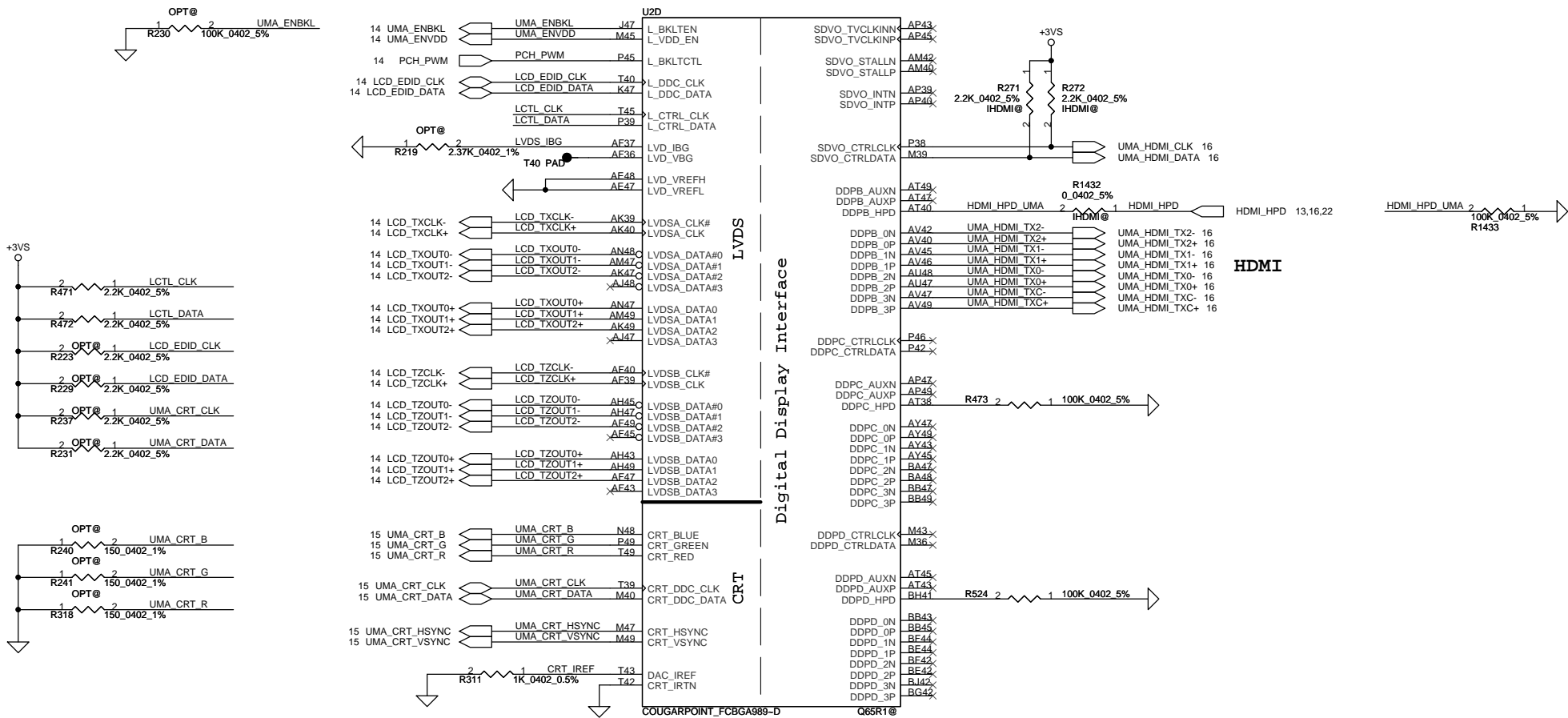


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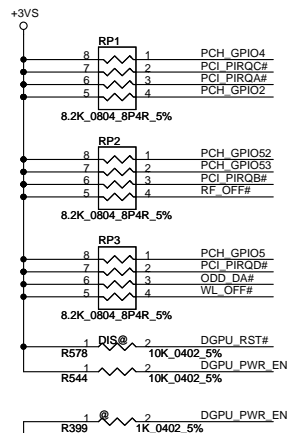




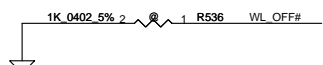
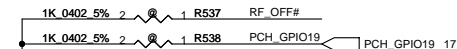
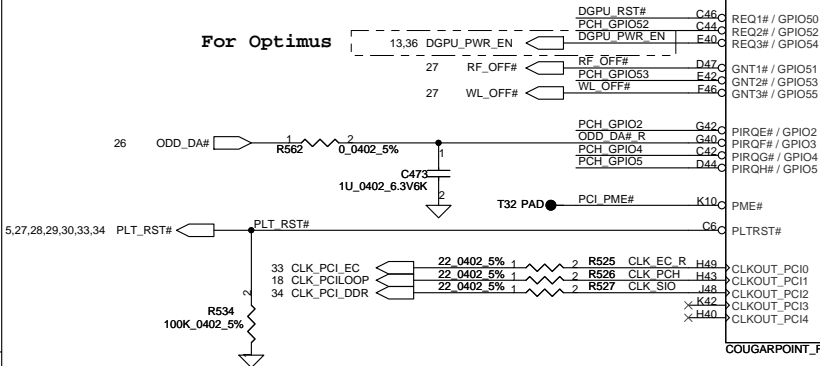




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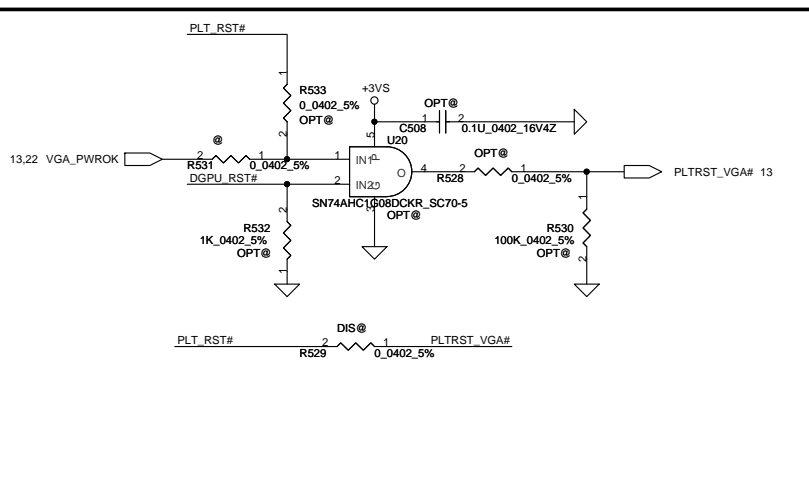
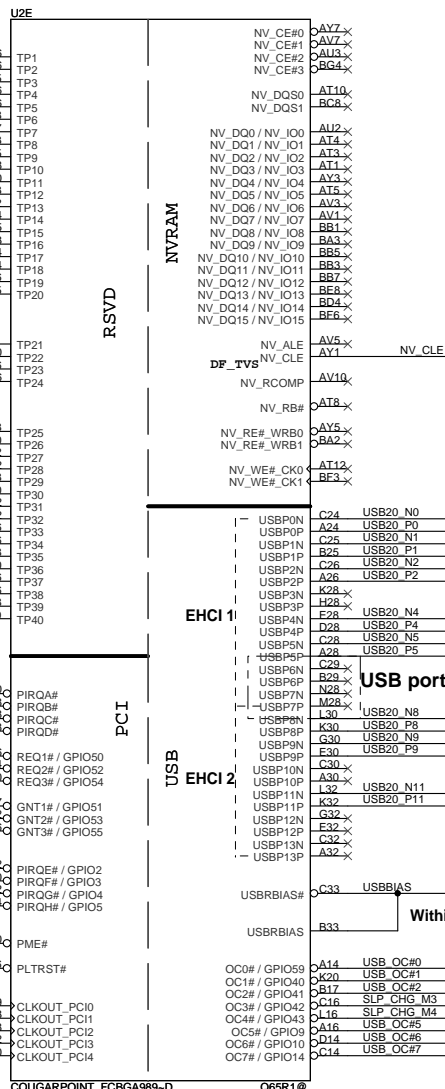


For Optimus



Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap	
WL_OFF#	Low= A16 swap override Enable High= A16 swap override Disable
*	



For Optimus

USB-RIGHT1
USB-RIGHT2
USB-Left1

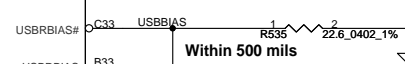
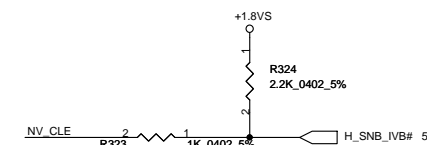
BlueTooth
IR Emitter

USB port6 and port7 are disabled on HM65

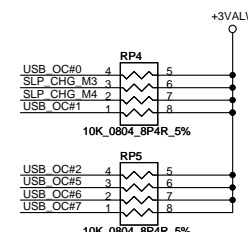
Finger Printer
WiMax

Int. Camera

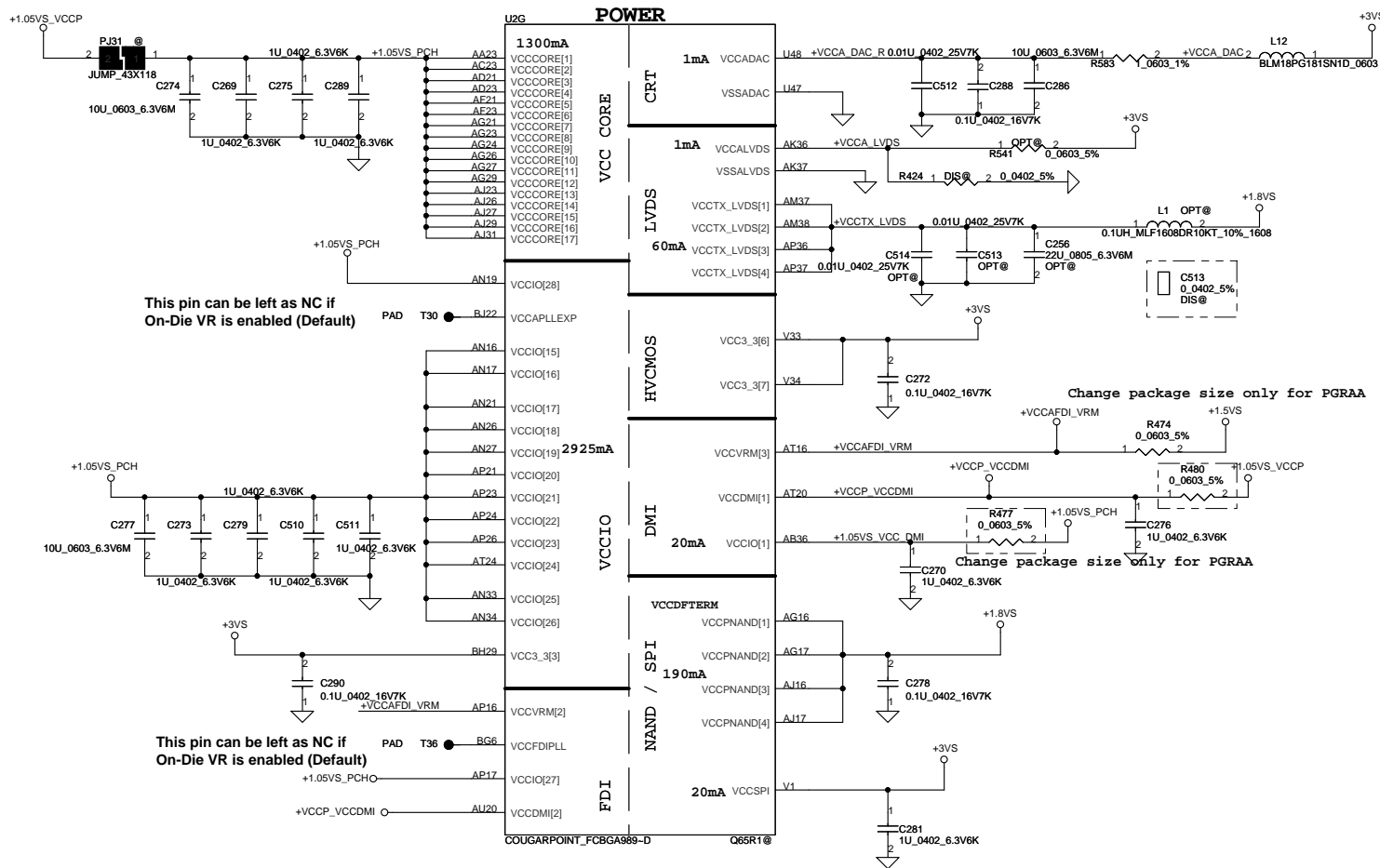
DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH Set to VSS when LOW



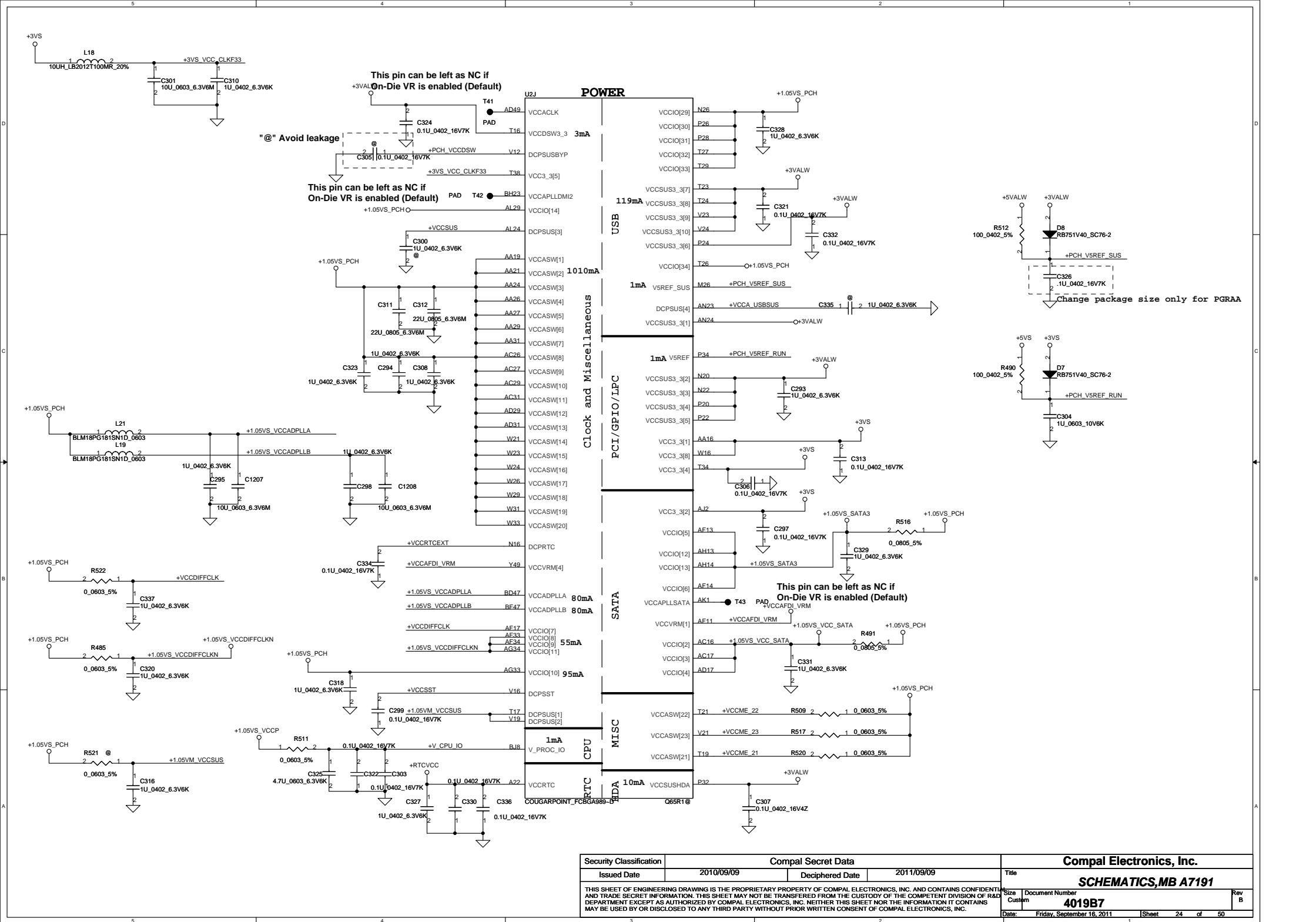
USB-Right
USB-Left

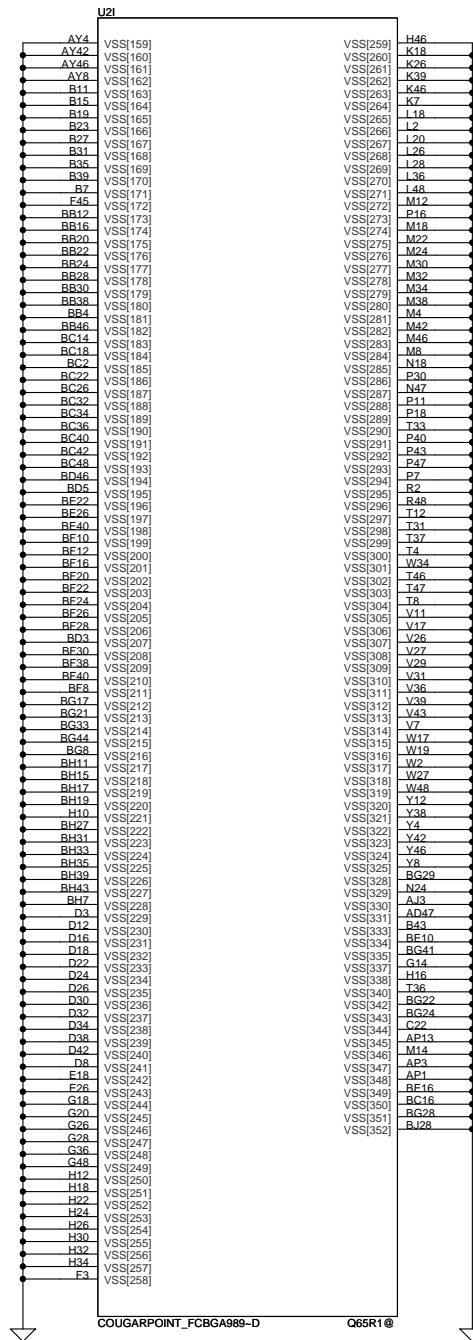
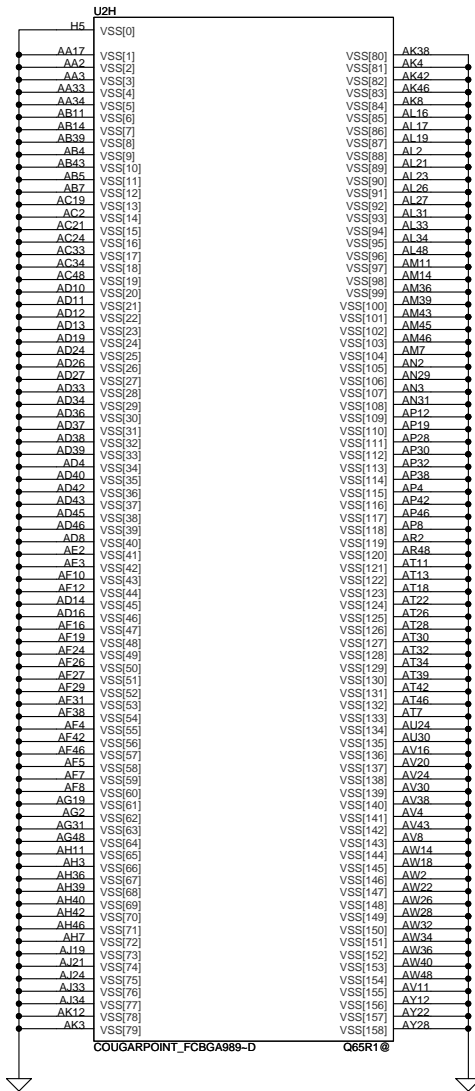


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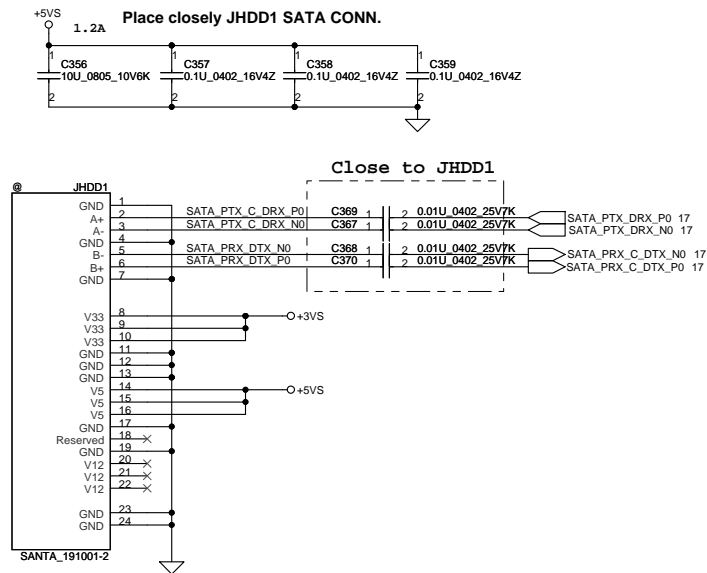
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLLA	1.05	0.08
VCCADPLLb	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTerm	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSusHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCCTX_LVDS	1.8	0.06



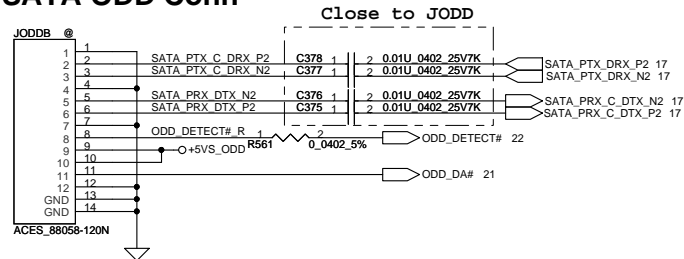


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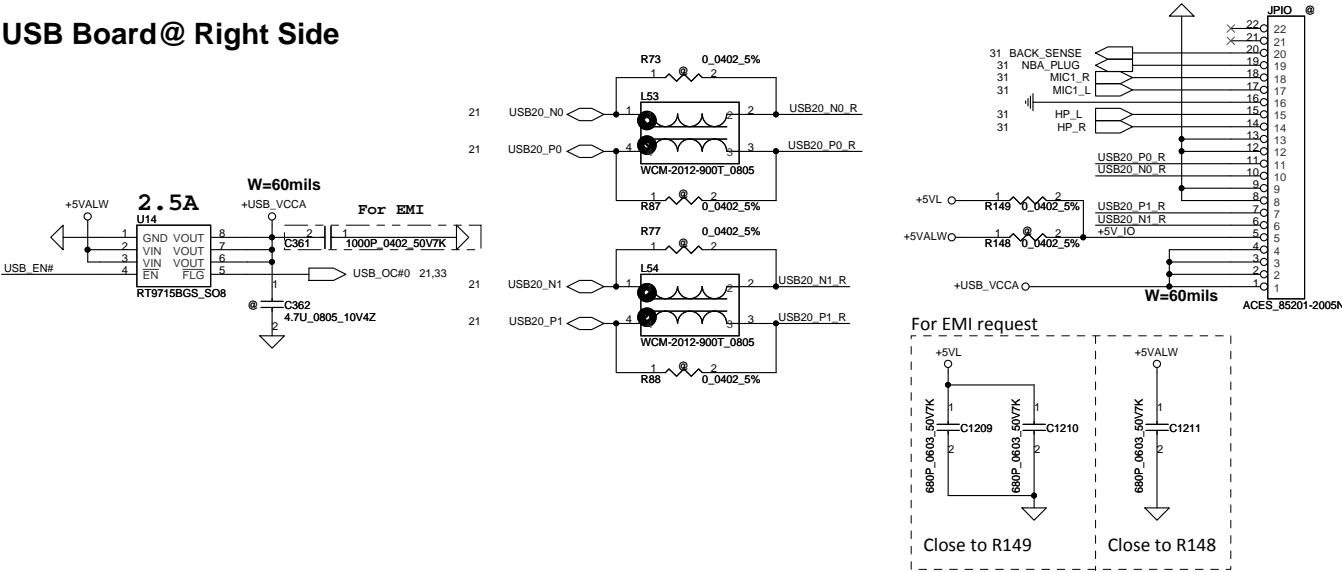
SATA Main HDD Conn.



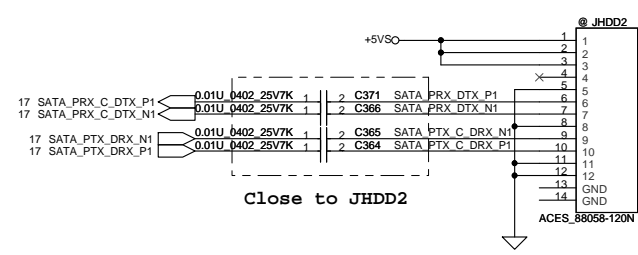
SATA ODD Conn



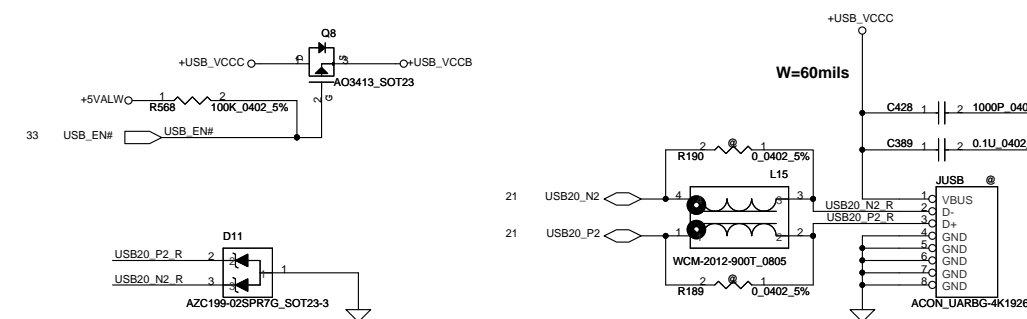
USB Board@ Right Side



SATA 2nd HDD Conn.

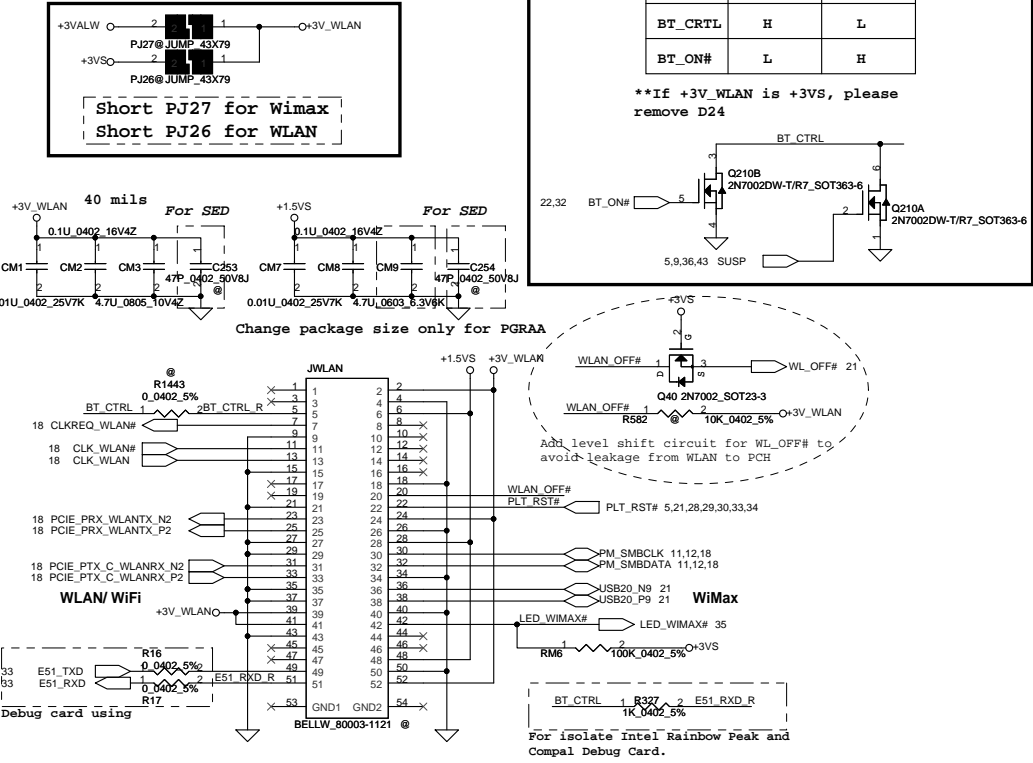


USB Board@ Left Side

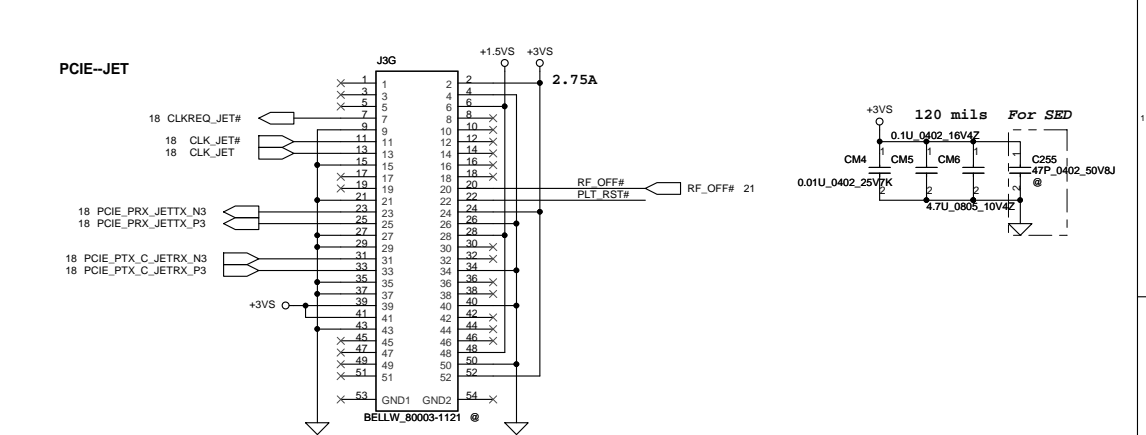


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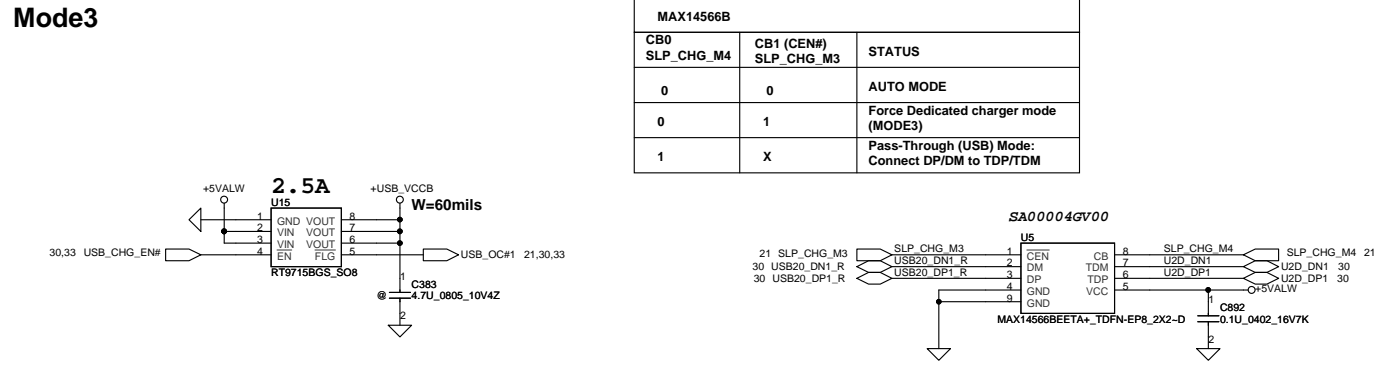
Slot 1 Half PCIe Mini Card-WLAN/ WiMax



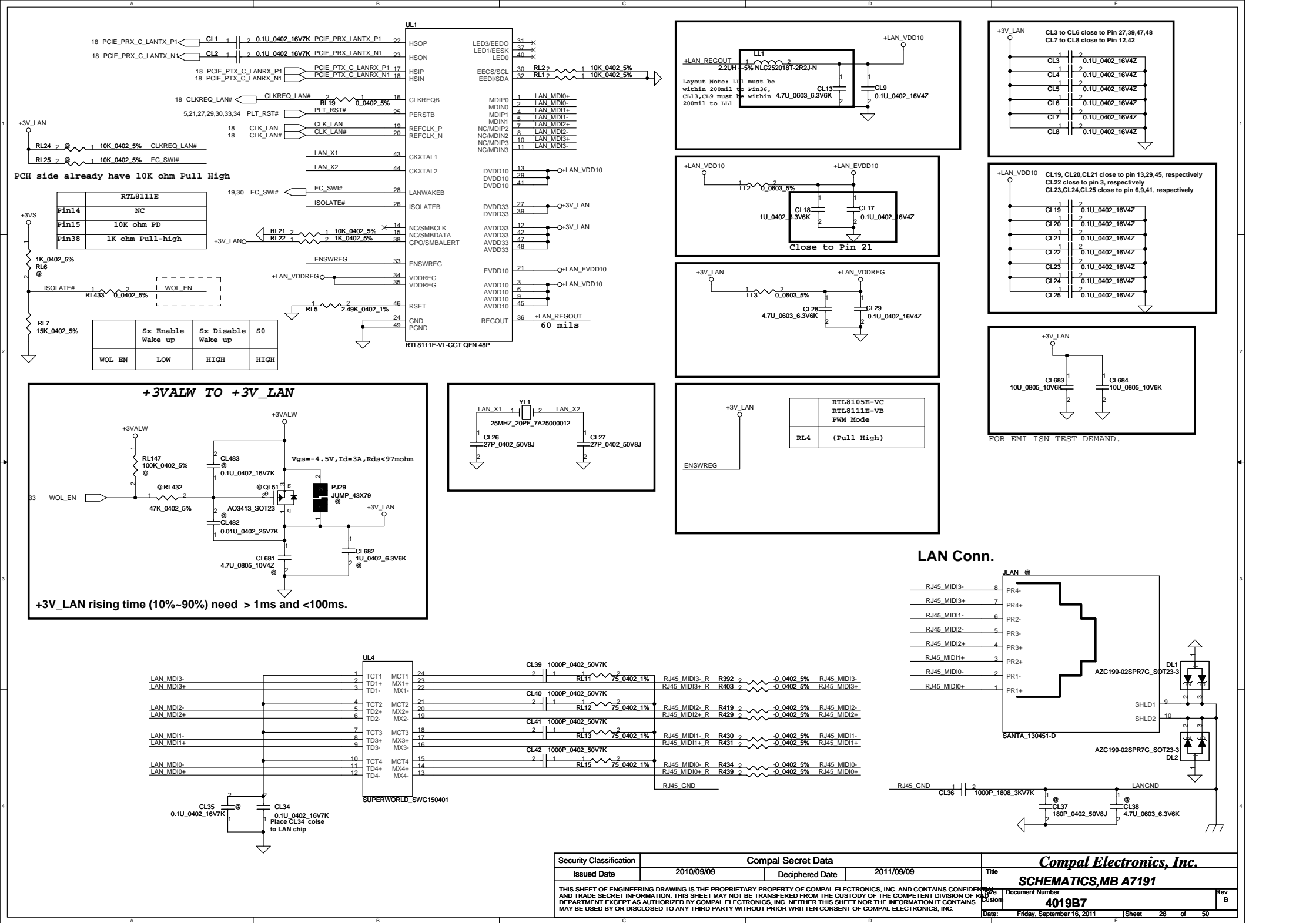
Slot 2 Half PCIe Mini Card- JET

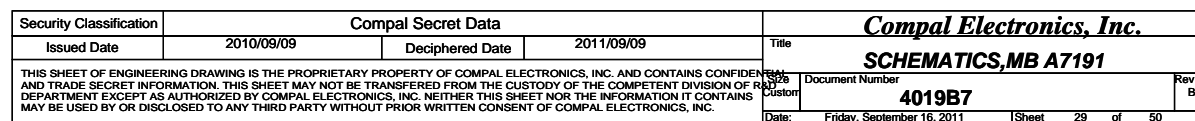


USB Sleep & Charge Auto-Mode Mode3

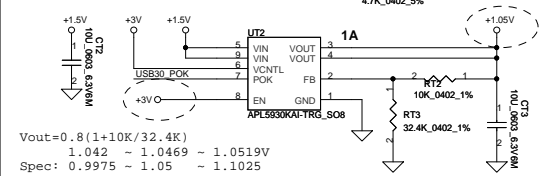


MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

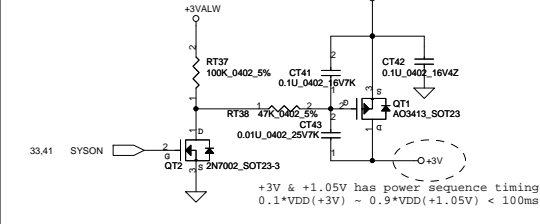




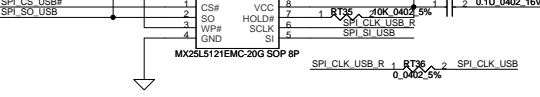
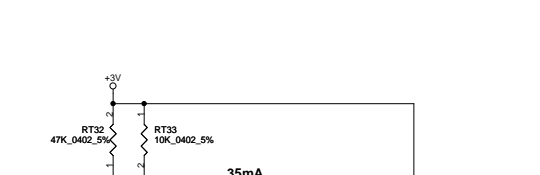
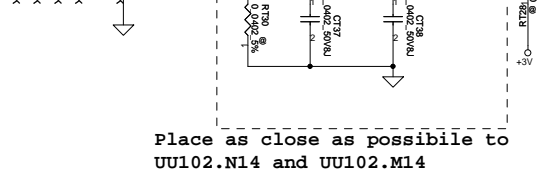
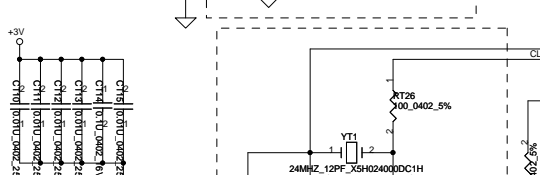
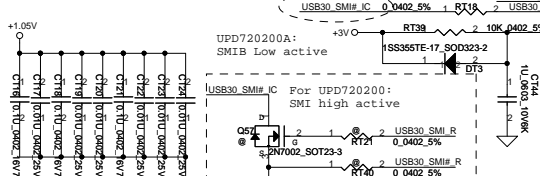
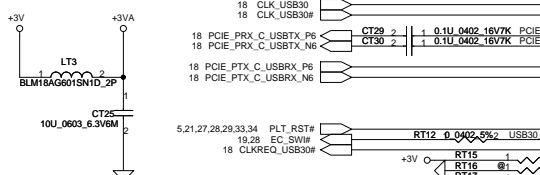
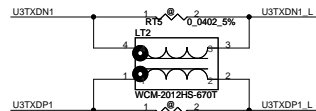
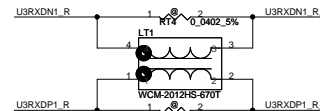
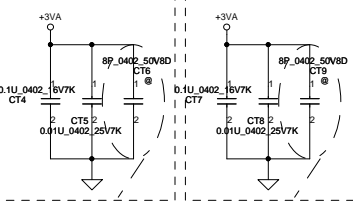
+1.5V to +1.05V Transfer



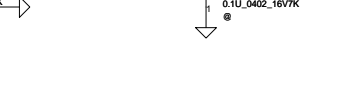
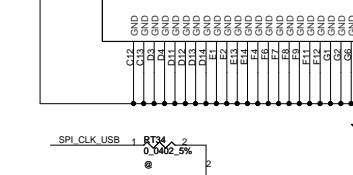
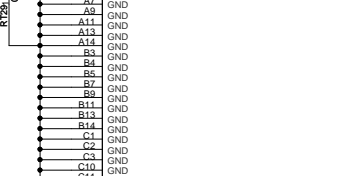
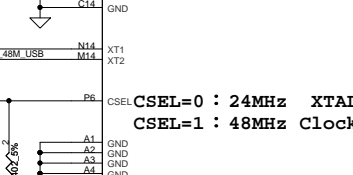
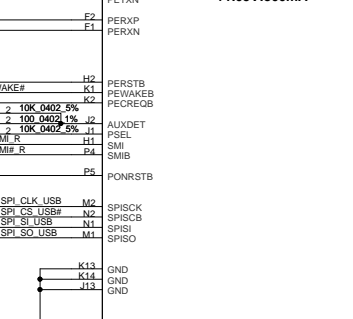
+3VALW to +3V Transfer



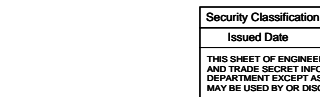
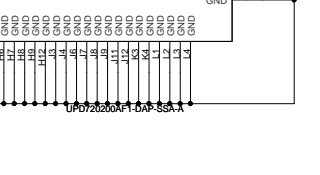
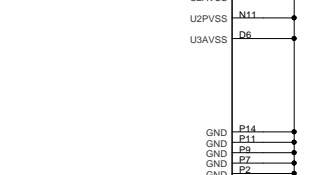
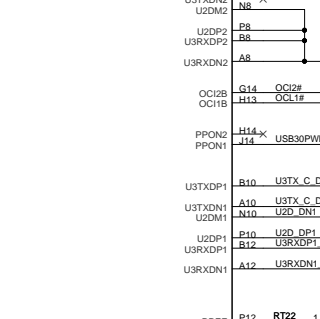
Close to U102.D7



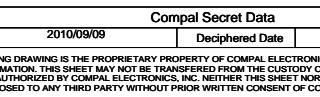
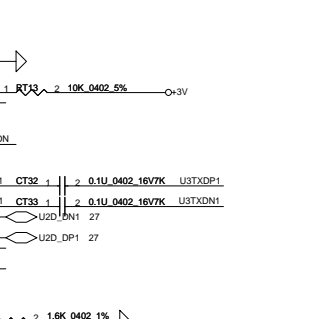
+3V:200mA +1.05V:800mA



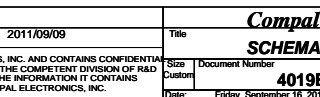
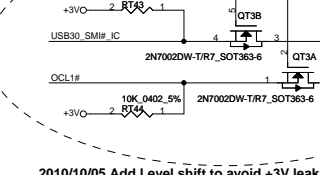
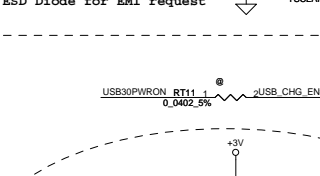
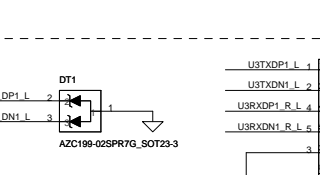
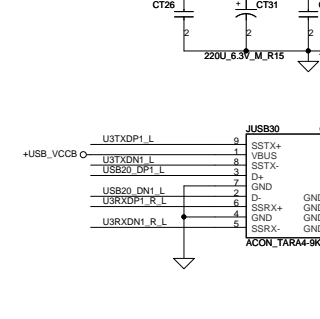
Close to U102.D7



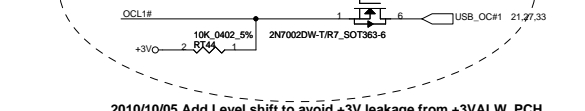
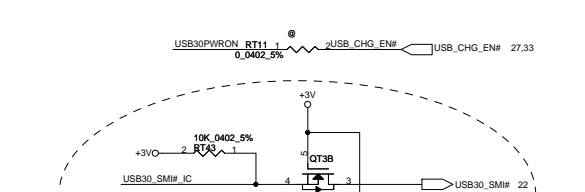
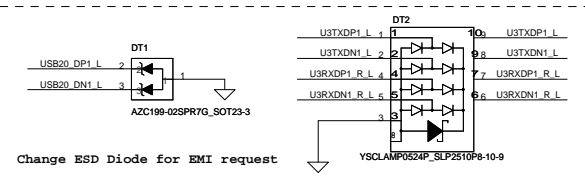
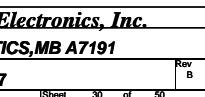
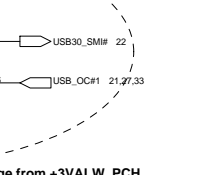
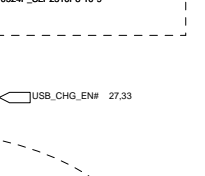
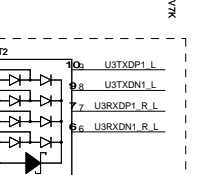
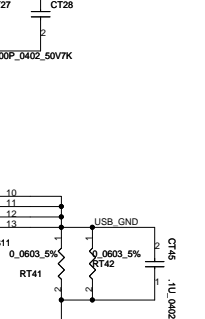
Close to U102.P13



Close to U102.D7



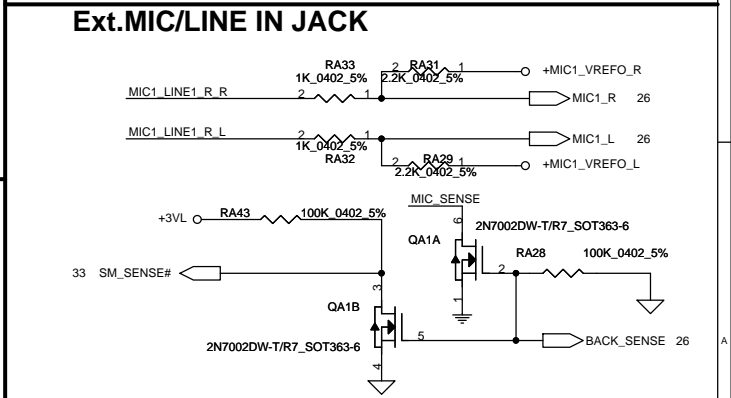
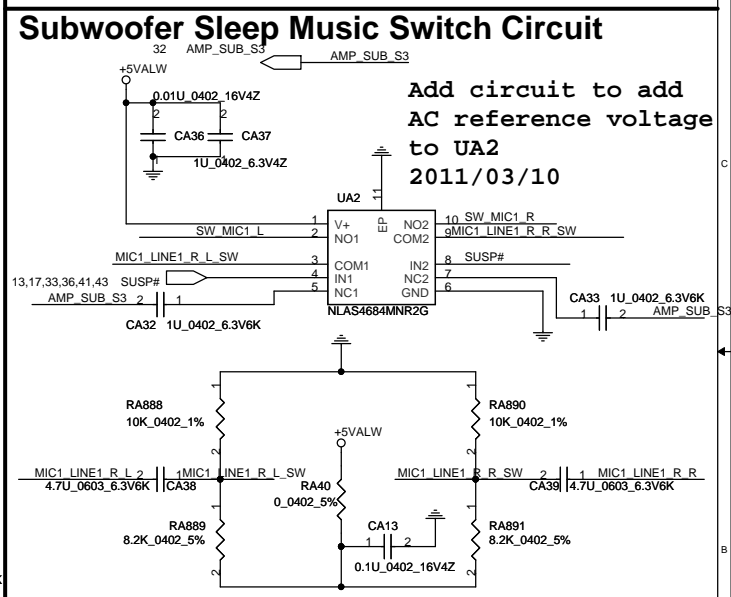
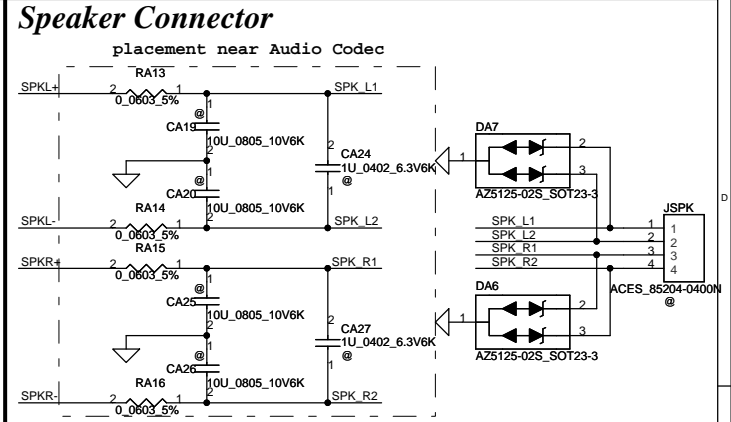
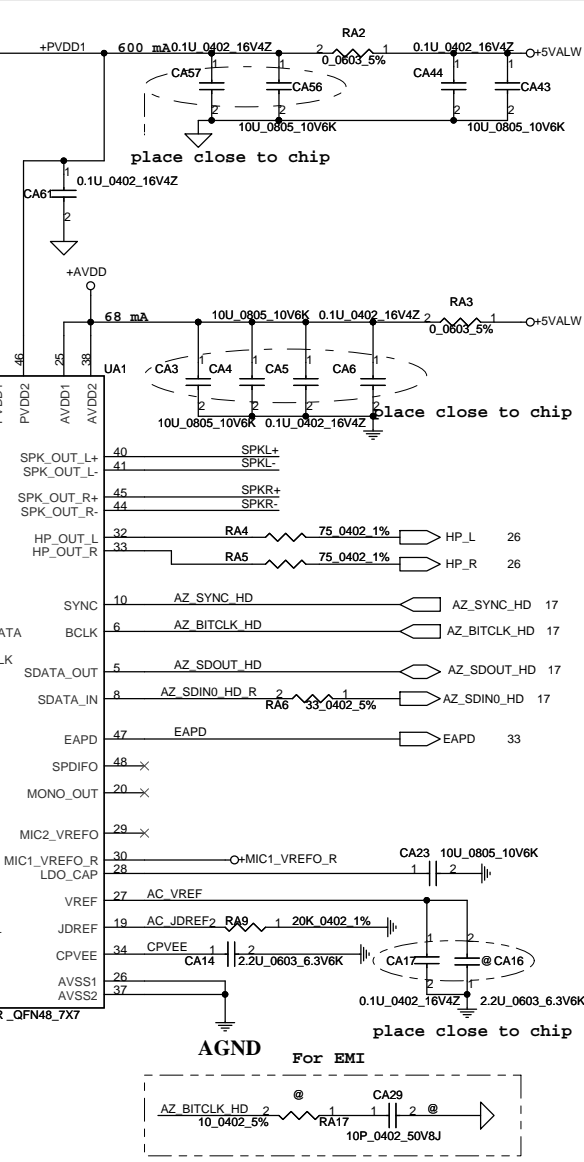
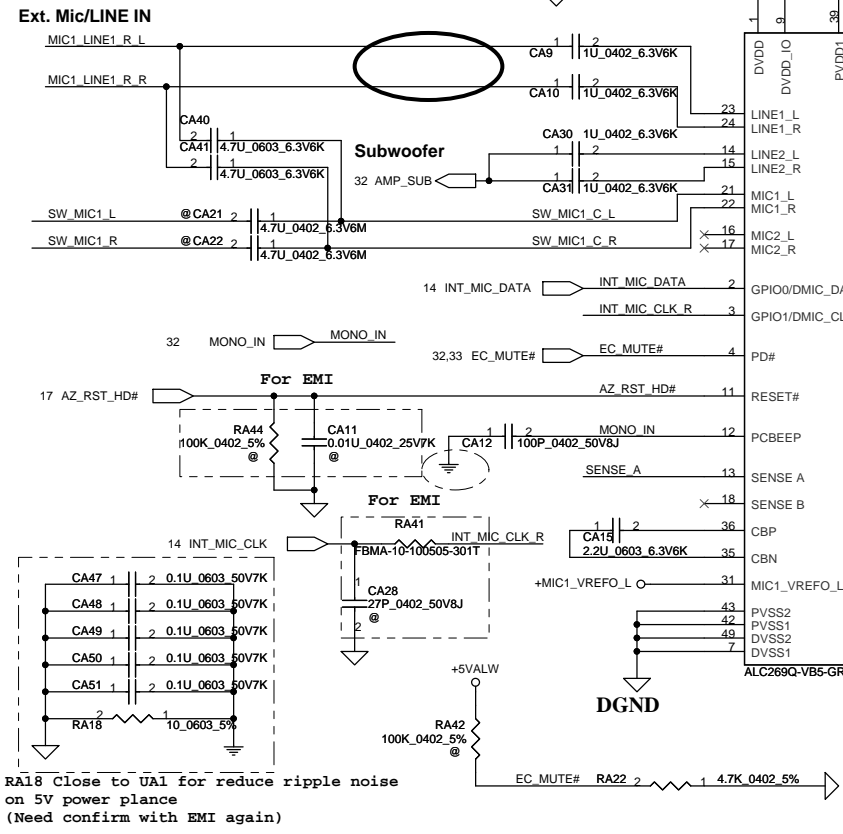
Close to U102.P13



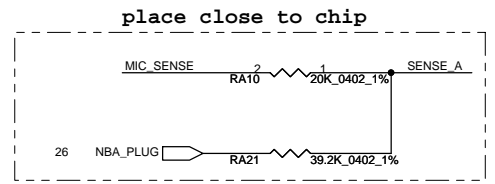
2010/10/05 Add Level shift to avoid +3V leakage from +3VALW_PCH

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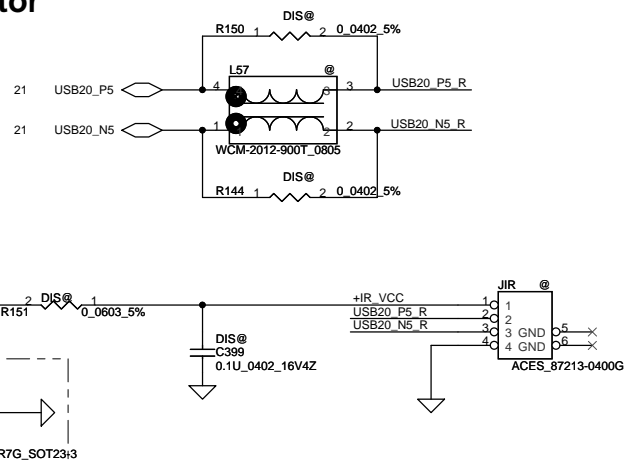
Delete resistor and
Capcitence for layout concern
2011/03/10



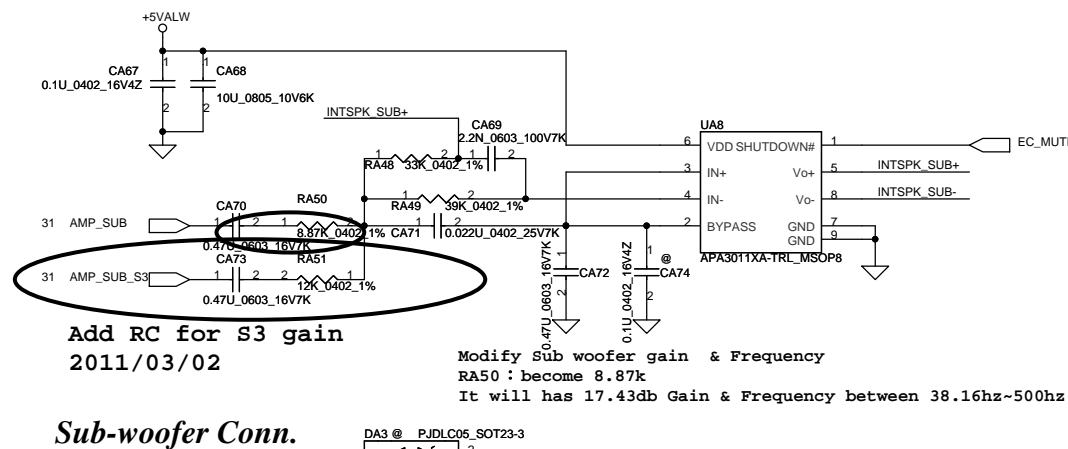
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



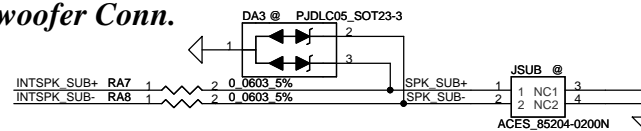
IR Emitter Connector



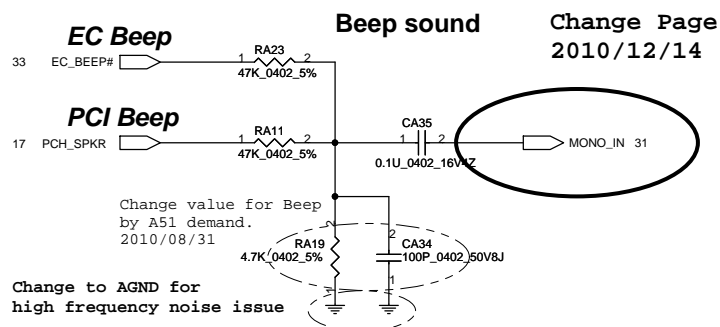
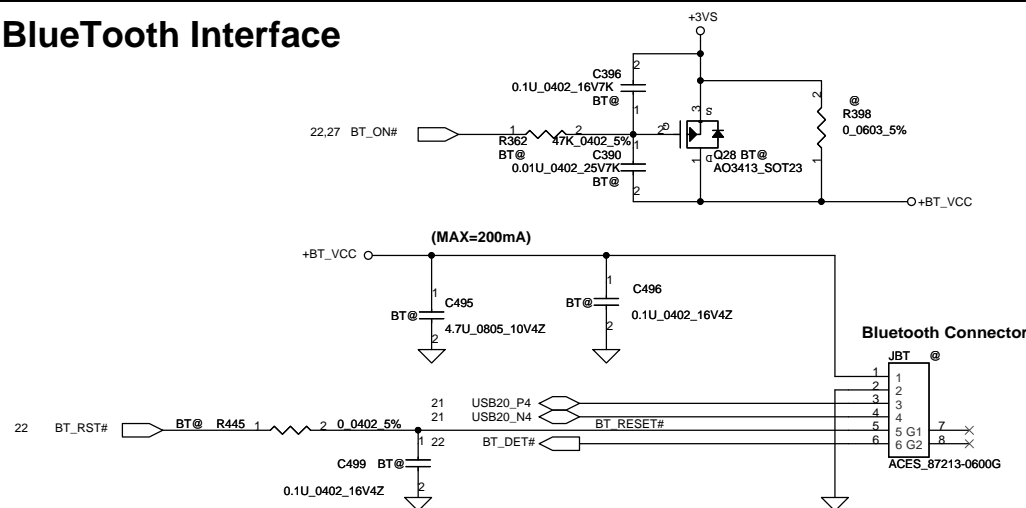
APA3011 Subwoofer Amplifier



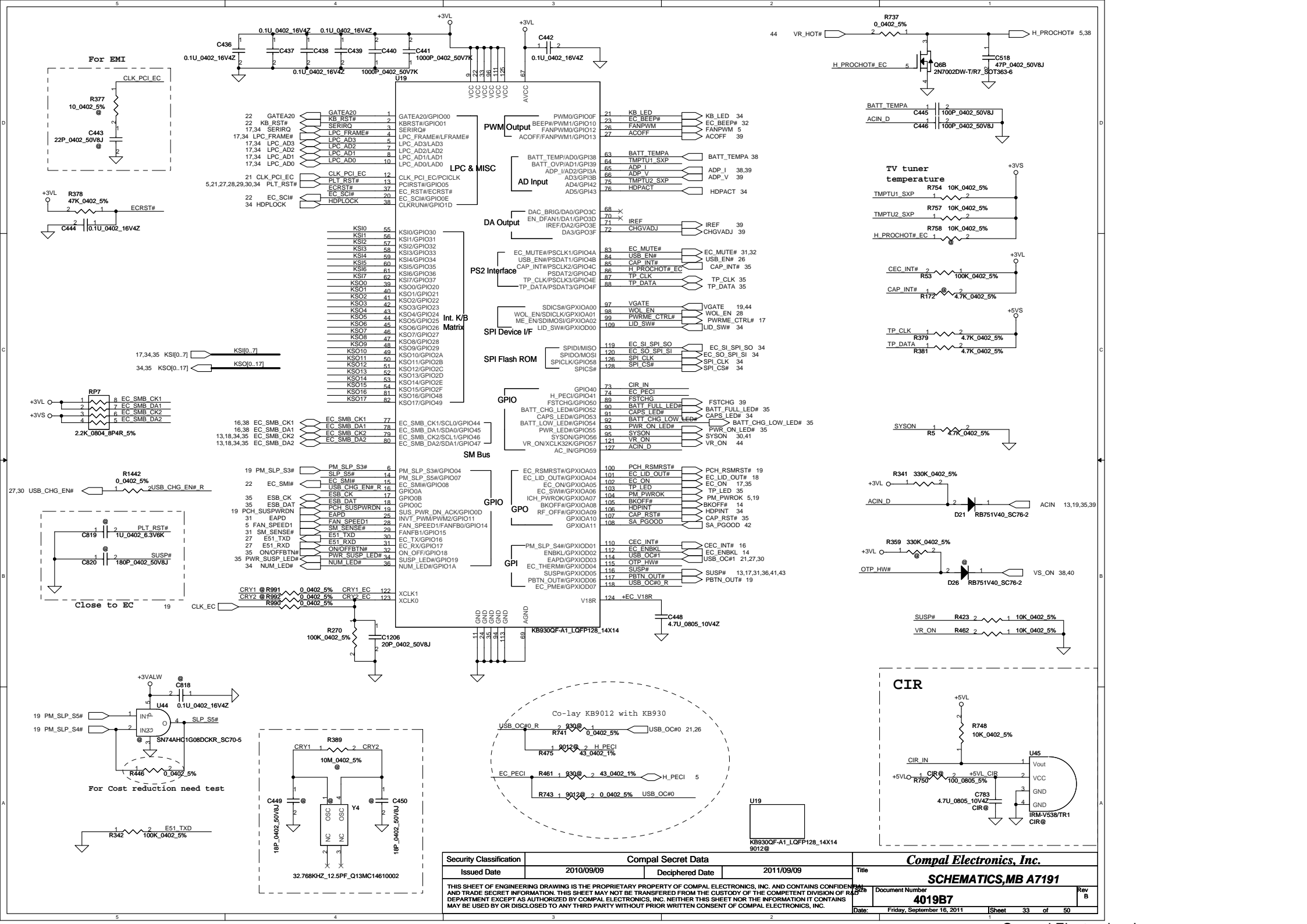
Sub-woofer Conn.



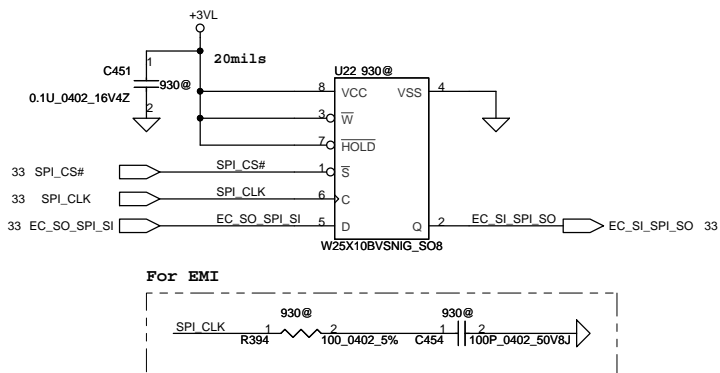
BlueTooth Interface



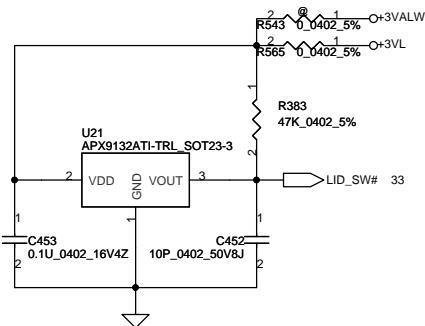
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SPI Flash (256KB)

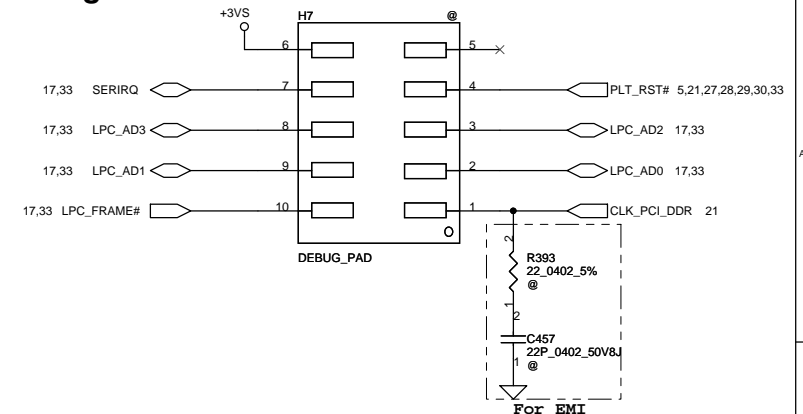


Lid SW

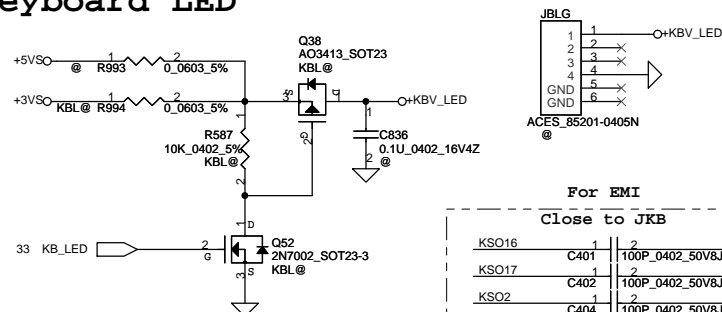


LPC Debug Port

Place the PAD under DDR DIMM.

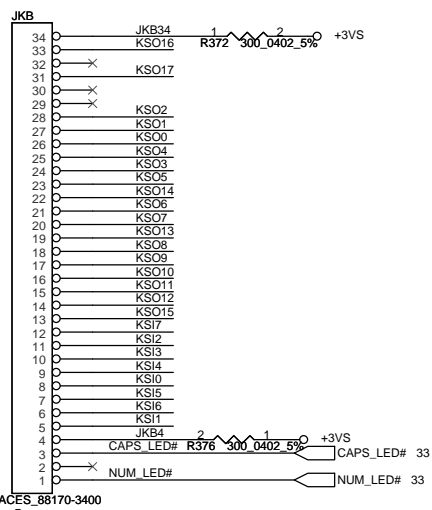


Keyboard LED



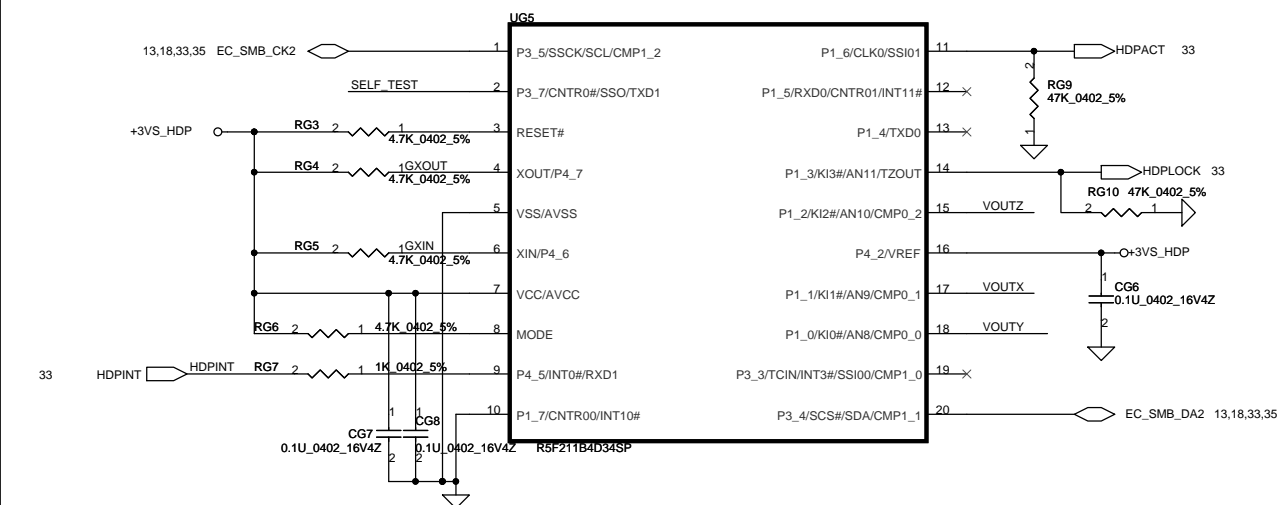
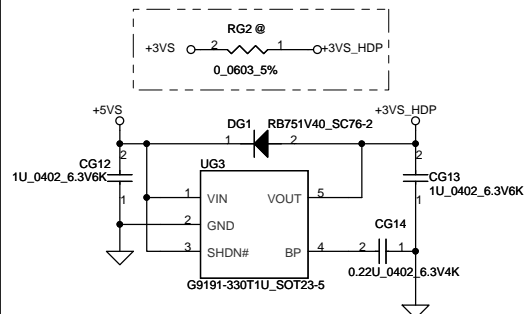
Notice: KB Connector Pin Definition
Reversed with KB Membrane Pin Definition

KEYBOARD CONN.



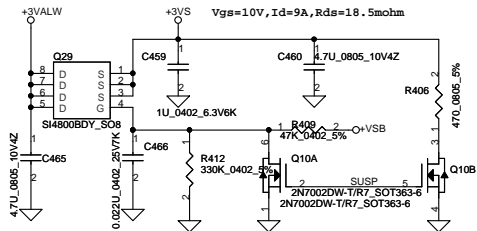
For EMI		
Close to JKB		
KSO16	C401	100P_0402_50VB/J
KSO17	C402	100P_0402_50VB/J
KSO2	C404	100P_0402_50VB/J
KSO1	C405	100P_0402_50VB/J
KSO0	C406	100P_0402_50VB/J
KSO4	C407	100P_0402_50VB/J
KSO3	C408	100P_0402_50VB/J
KSO5	C409	100P_0402_50VB/J
KSO14	C410	100P_0402_50VB/J
KSO6	C411	100P_0402_50VB/J
KSO7	C412	100P_0402_50VB/J
KSO13	C413	100P_0402_50VB/J
KSO8	C415	100P_0402_50VB/J
KSO9	C416	100P_0402_50VB/J
KSO10	C417	100P_0402_50VB/J
KSO11	C418	100P_0402_50VB/J
KSO12	C419	100P_0402_50VB/J
KSO15	C420	100P_0402_50VB/J
KSI7	C421	100P_0402_50VB/J
KSI2	C422	100P_0402_50VB/J
KSI3	C423	100P_0402_50VB/J
KSI4	C424	100P_0402_50VB/J
KSI0	C425	100P_0402_50VB/J
KSI5	C427	100P_0402_50VB/J
KSI6	C429	100P_0402_50VB/J
KSI1	C431	100P_0402_50VB/J
CAPS LED#	C433	100P_0402_50VB/J
NUM LED#	C435	100P_0402_50VB/J

G-Sensor

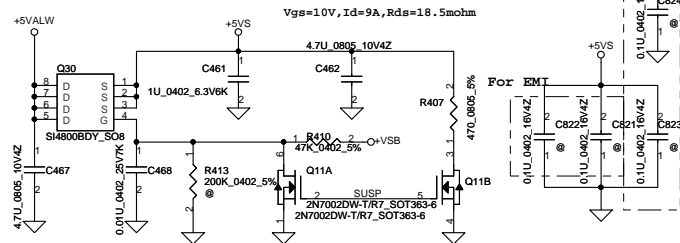


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+3VALW TO +3VS

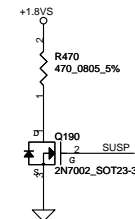
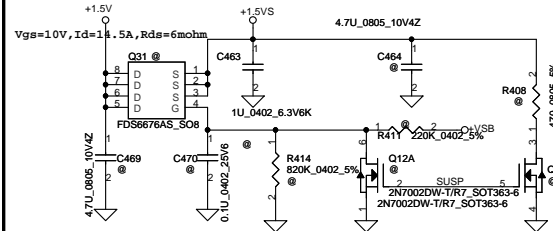


+5VALW TO +5VS

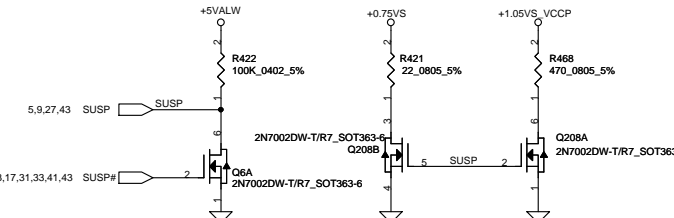
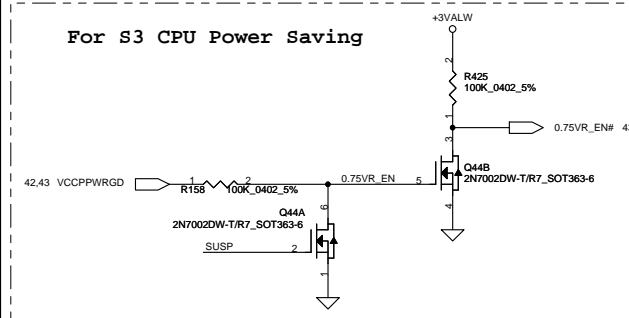


+1.5V to +1.5VS

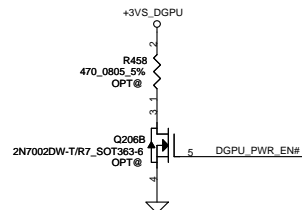
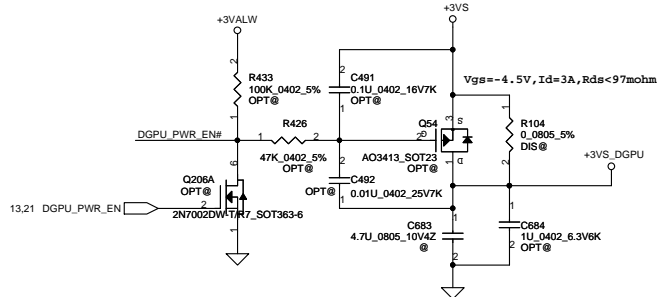
Unmount below part for cost down plan
2010/12/23



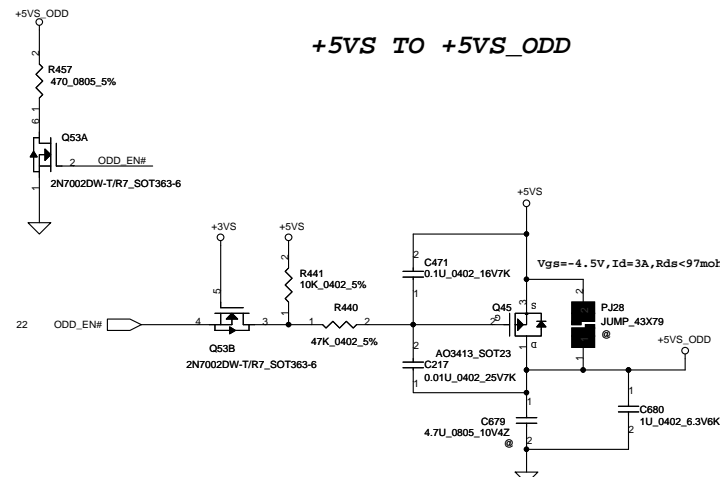
For S3 CPU Power Saving



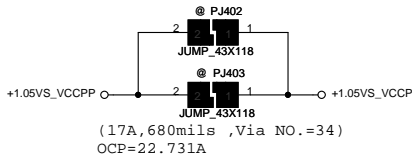
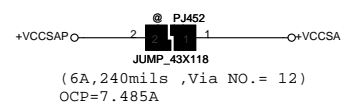
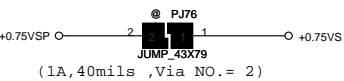
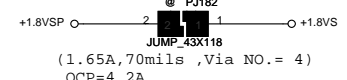
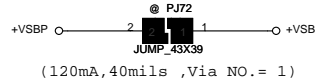
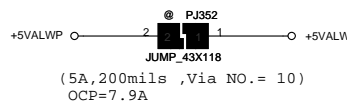
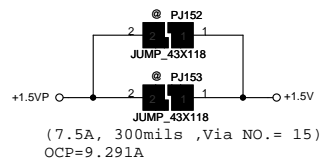
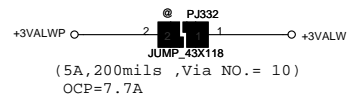
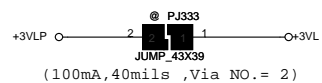
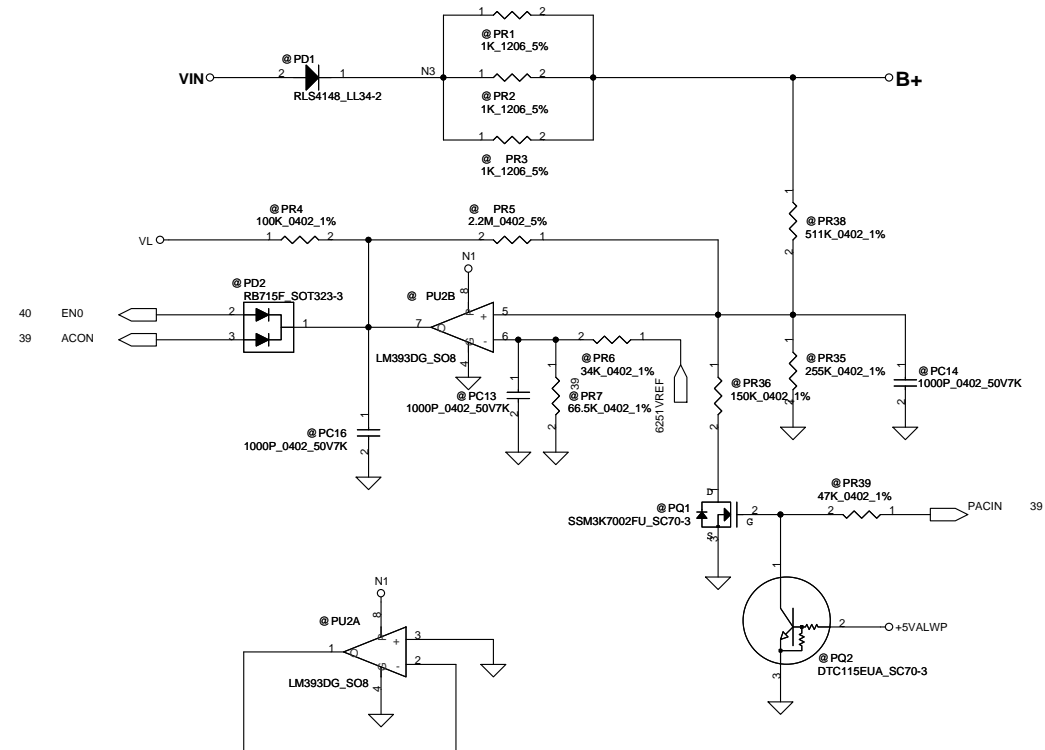
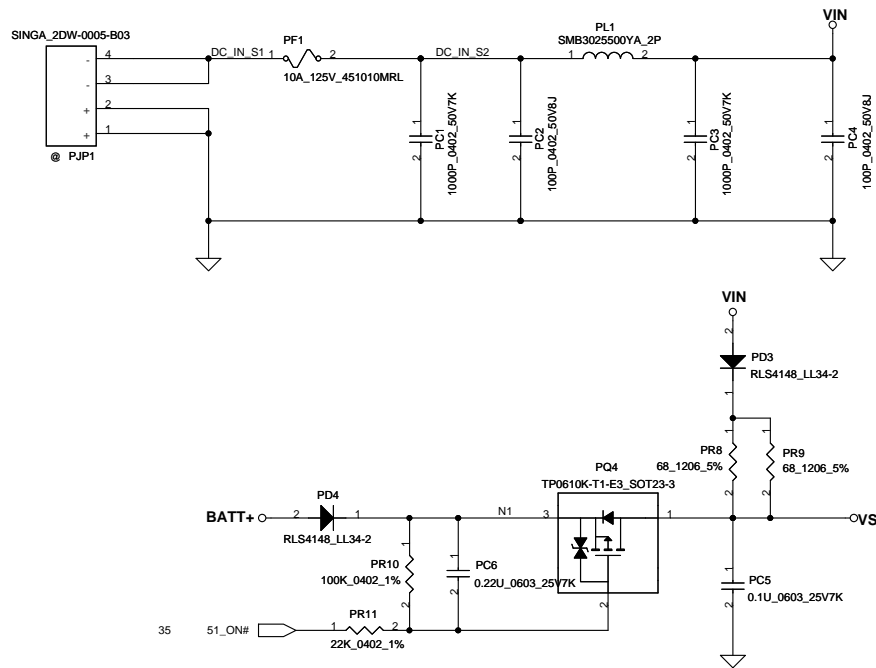
+3VS to +3VS_DGPU



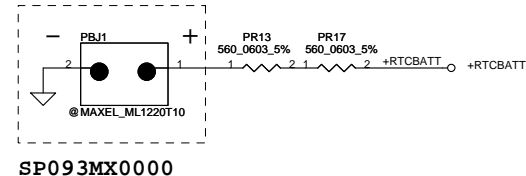
+5VS TO +5VS_ODD



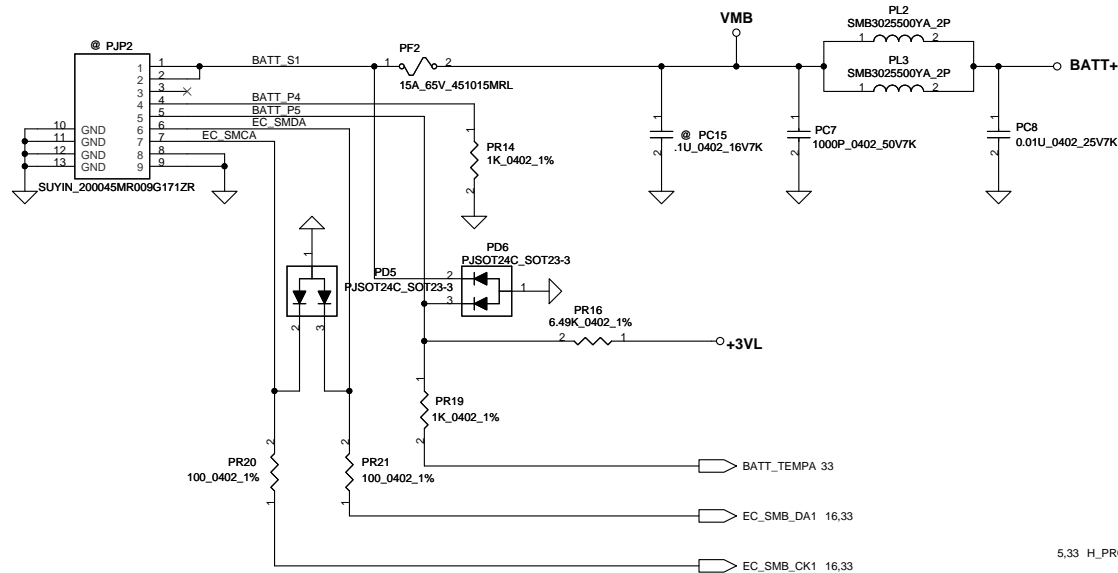
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RTC Battery



ACIN			
Precharge detector			
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V



PH1 under CPU botten side :

CPU thermal protection at 90 degree C

Recovery at 56 degree C

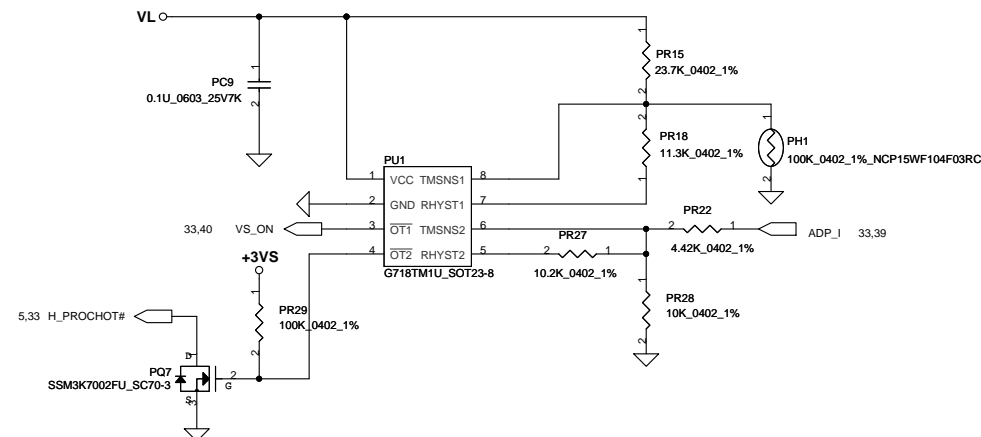
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

$$R_{tmh} \text{ at } 90C = 7.87K, R_{tml} \text{ at } 56C = 26.1K$$

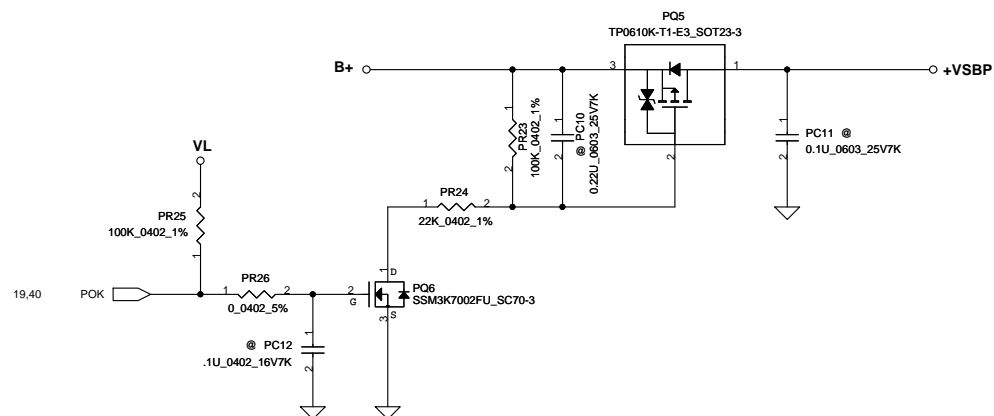
$$R_{set} = 3 * 7.87K = 23.61K \Rightarrow 23.7K$$

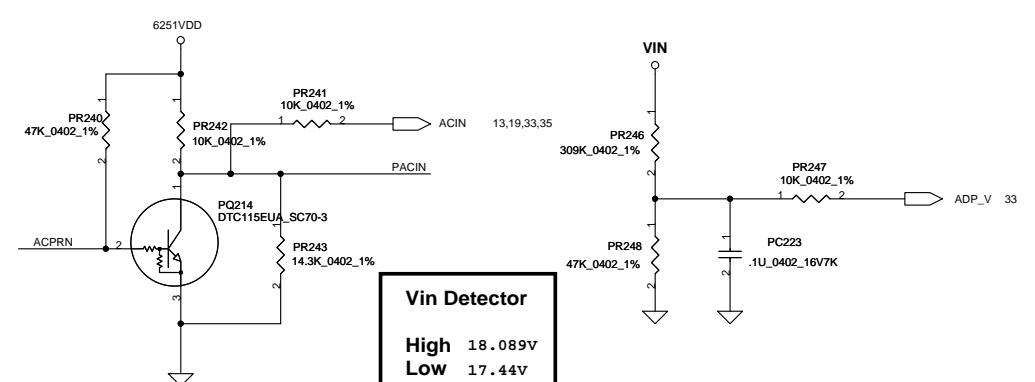
$$R_{hyst} = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K \Rightarrow 11.3K$$



Adaptor protection

Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
180W	224W	2.34V	172W	1.80V

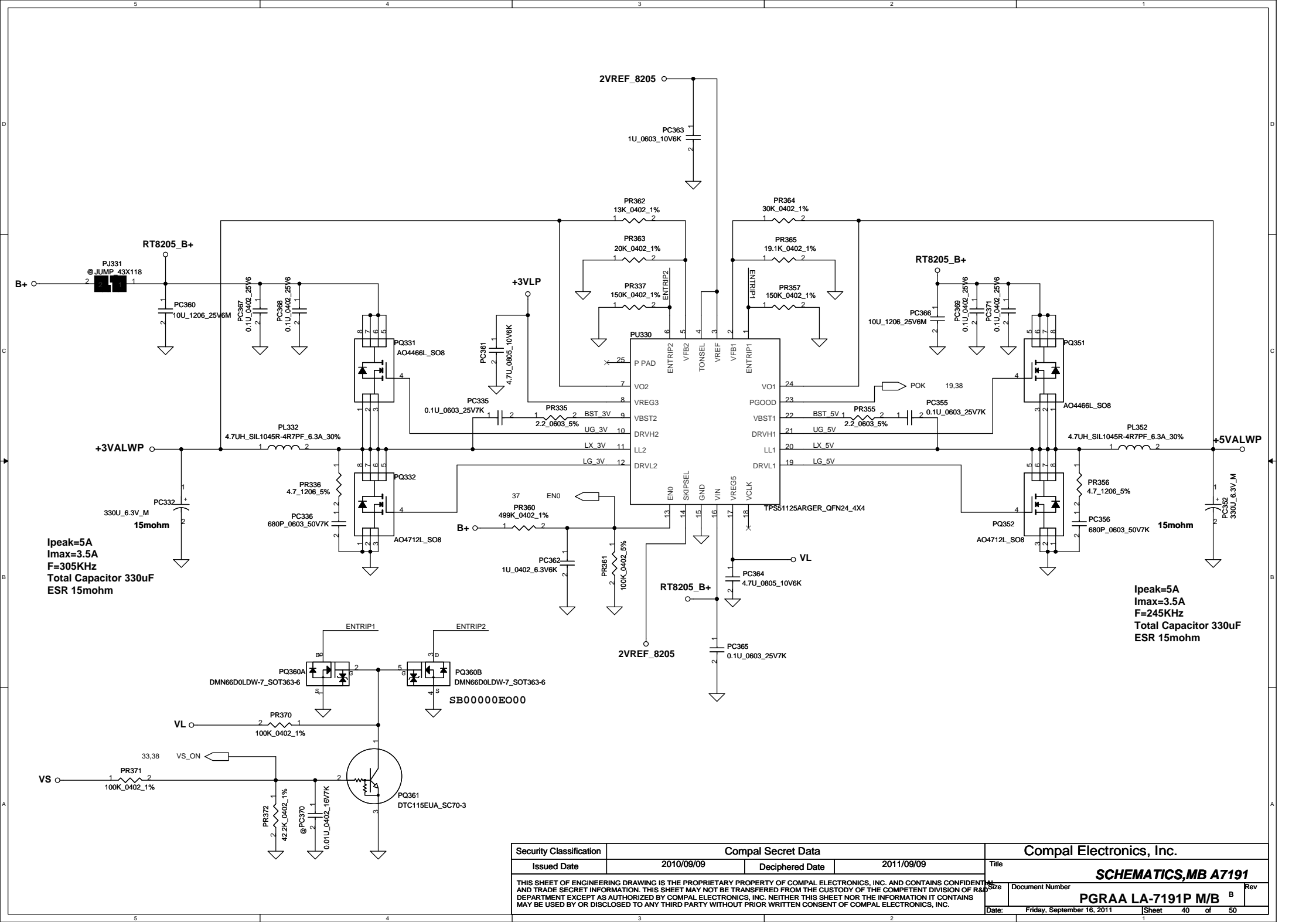




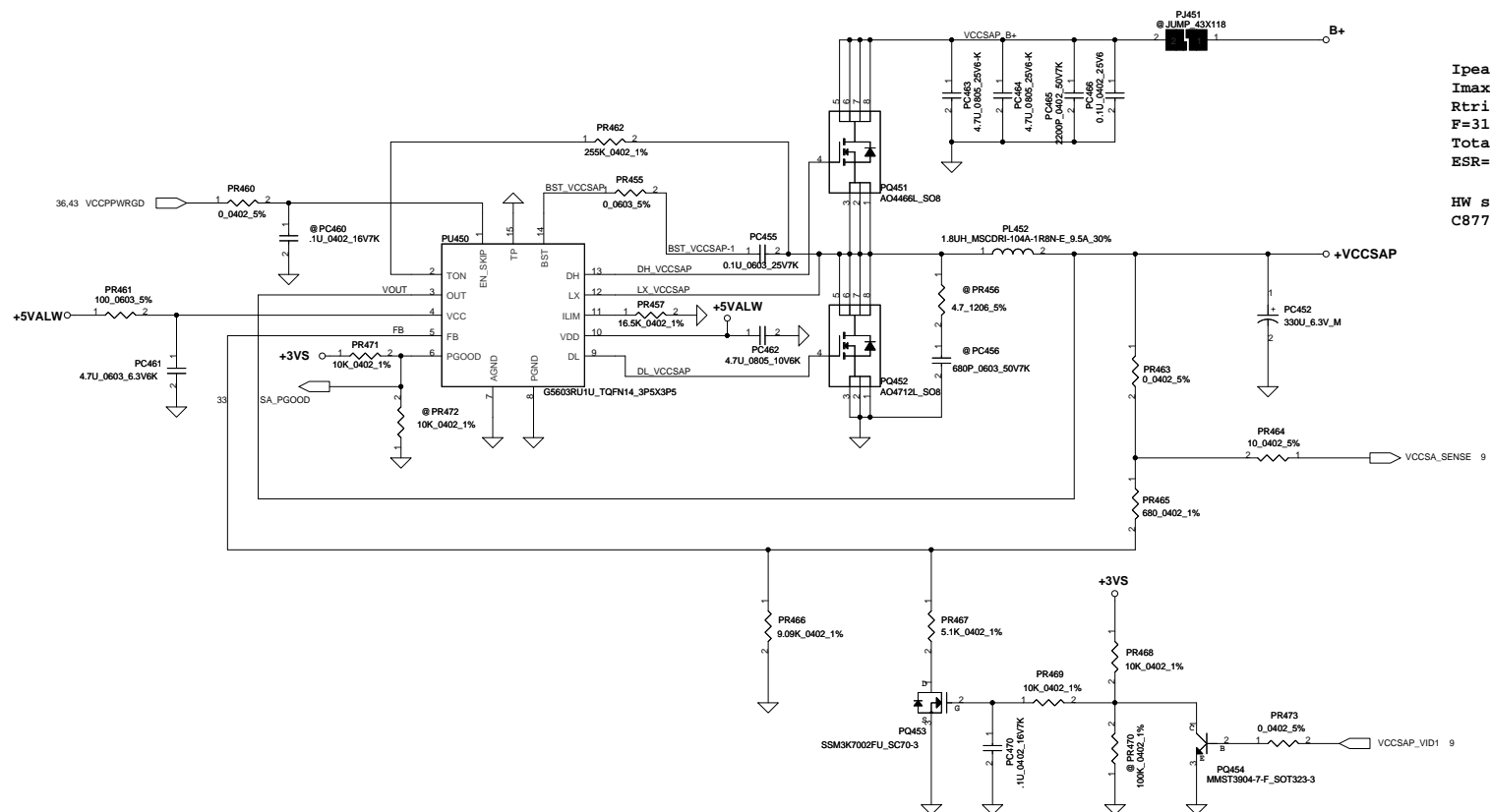
CP mode CP= 92%*Iada

Iada=0~3.42A(65W)	CP=3.147A	
Vaclim=0.6221V(65W)	PR222=75k,	PR223=20k, PR215=0.02
Iada=0~3.947A(75W)	CP=3.63A	
Vaclim=1.1V(75W)	PR222=24k,	PR223=20k, PR215=0.02
Iada=0~4.737A(90W)	CP=4.36A	
Vaclim=0.737V(90W)	PR222=53.6k,	PR223=20k, PR215=0.015
Iada=0~6.316A(120W)	CP=5.81A	
Vaclim=1.777V(120W)	PR222=8.25k,	PR223=26.7k, PR215=0.015
Iada=0~9.47A(180W)	CP=8.72A	
Vaclim=1.779V(180W)	PR222=24k,	PR223=100k, PR215=0.01

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Ipeak=6A
 Imax=4.2A
 Rtrip=16.5K, OCP=7.485A
 F=315KHz
 Total Capacitor 330u
 ESR=15mohm

HW side:
 C877 330uF 17m @; C485 330uF 6m @

VID1	+VCCSAP
1	0.8V
0	0.9V

Reserve PC574, PR552
for slow rate

If HW side have add resistor PWR
side can remove PR129, PR130

Connect to +5V can disable GFX portion,
but PR575 need to be removed.

Reserve PC559, PR550
for slow rate

If HW side have add resistor PWR
side can remove PR131, PR132

+CPU_CORE
I_ocp=120A, I_{cc}MAX=94A
Load line=1.9mohm
DCR=1.1mohm

+GFX_CORE
I_ocp=40A, I_{cc}MAX=33A
Load line=3.9mohm
DCR=1.1mohm

quad core

+CPU_CORE
I_ocp=70A, I_{cc}MAX=53A
Load line=1.9mohm
DCR=1.1mohm

+GFX_CORE
I_ocp=40A, I_{cc}MAX=24A
Load line=3.9mohm
DCR=1.1mohm

dual core

Security Classification

Compal Secret Data

Compal Electronics, Inc.

Issued Date

2010/09/09

Deciphered Date

2011/09/09

Title

SCHEMATICS, MB A7191

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Document Number

PGRAA LA-7191P M/B

Date

Friday, September 16, 2011

Sheet

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of

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE																																														

EVT --> DVT																																																		
1	2010/11/7	P39	change PL201 1.2uH(SH000000B100) to 1uH(SH000000MN00)	cost down																																														
2	2010/11/7	P41	change PR157 SD0341622YT to SD034162280	previous P/N is for carPC use																																														
3	2010/11/7	P37	change precharge to unmount	reserve precharge																																														
4	2010/11/7	P39	change PQ203, PQ204 from AO4407A to AO4409L	higher curretn withstanding ability																																														
5	2010/11/7	P39	change PR219 from 47K to 100ohm	prevent ADP_I from being divided																																														
6	2010/11/7	P37	change PJP3 to PJP1	wrong name																																														
7	2010/11/16	P39	charger pin4 pull high VDD	4 cells design should pull high VDD																																														
8	2010/11/16	P38	change PR27 to 10.2K	set adaptor protection power to 224W																																														
9	2010/11/16	P44	change PR551 to 3.65K	adjust CPU_CORE loadline																																														
10	2010/11/16	P38	change PD5, PD6 to SCA00000W00	follow ESD team suggestion main source																																														
11	2010/11/16	P39	change PR215=0.01ohm, PR222=24K, PR223=100K	change adaptor power to 180W																																														
12	2010/11/19	P44	change PC551 to mount	adjust CPU_CORE transient waveform																																														
13	2010/11/19	P44	change PL502, 503, 504, 505 foot print to MAG_MMD10DZR36MS1_4P	to solve poor solder issue																																														
14	2010/11/19	P41	change PL182 to SH000000KS00	original TMP choke is forbidden																																														
15	2010/11/19	P41	mount PR156, PC156; change PR155 to 2.2ohm	EMC request																																														
16	2010/11/19	P44	mount PR516, PR526, PR536, PC516, PC526, PC536; change PR515, PR525, PR535 to 2.2ohm	EMC request																																														
17	2010/11/19	P44	add PC589, PC590 0.1uF 0402	EMC request																																														
18	2010/11/26	P44	PR567 change to 24.9K, unmount	set GFX Imax register to 33A																																														
19	2010/11/26	P38	add PL3 bead	add design margin for battery current on this bead																																														
20	2010/12/3	P39	mount PC207, PC208, PC209	EMC request																																														
DVT1 --> DVT2																																																		
21	2011/1/14	P44	modify PR550 part number to SD034200180	previous part number is wrong																																														
22	2011/1/14	P42	change PR461 to 0603, PC461 to 0603	change to common size																																														
23	2011/1/14	P44	modify PC549 to 25V (SE0000005Z80)	previous 10V is wrong																																														
24	2011/1/14	P39	modify PQ208, PQ209 to AO4407AL	change to L																																														
25	2011/1/14	P44	change PC551 to unmount	adjust CPU_CORE transient waveform																																														
26	2011/1/19	P44	change PC571 to 47nF, PC573 to 33nF	adjust GFX_CORE transient waveform																																														
27	2011/1/19	P44	change PR534 to 2.8K, PR575 to 680	adjust GFX_CORE loadline and OCP																																														
DVT2 --> PVT																																																		
28	2011/2/18	P42	modify PL452 to SH0000008U80	can use higher height choke																																														
29	2011/2/18	P43	modify 1.05V Rtrip PR407 to 7.15K	recalculte OCP to 21.3A																																														
30	2011/2/18	P43	modify 1.05V Vout PC402 to 390uF	for OVP design requirement																																														
31	2011/2/18	P39	change PL202 charger choke to 7*7 molding M600	layout replacement requirement																																														
32	2011/2/25	P37	change PJP1 + - pin define	for power switch relocation layout replacement																																														
33	2011/3/2	P37	delete GFX_CORE jump PJ502, PJ503	for save space																																														
37	2011/3/7	P40	change PR335 and PR355 to 2.2ohm (boost resistor) add 3/5V snubber circuit, PR336, PC336, PR356, PC356	EMI request																																														
38	2011/3/7	P40	add 0.1uF caps, PC367, PC368, PC369, PC371 at 3/5V B+	EMI request																																														
39	2011/3/10	P44	add 10uF 1206 (PC575, PC576, PC577, PC578, PC579) at CPU_B+ and B+	EMI request																																														
40	2011/3/14	P43	change PR406, PC406(snubber circuit) to mount, PR405 to 2.2ohm(Rboost)	to solve enter system hang up issue, reduce 1.05V noise																																														
PVT --> PreMP																																																		
41	2011/4/4	P39	change PR236 : 47K to 200K, PR237 : 10K to 47K	design change																																														
42	2011/4/20	P41	change PR157 to 20K	OCP design change																																														
43	2011/4/20	P42	change PR457 to 16.5K	OCP design change																																														
44	2011/4/20	P43	change PR407 to 8.87K	OCP design change																																														
<table><tr><td colspan="2">Security Classification</td><td colspan="2">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td colspan="2">Issued Date</td><td colspan="2">2010/09/09</td><td colspan="2">Deciphered Date</td><td colspan="2">2011/09/09</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td colspan="2">Title</td><td colspan="2">SCHEMATICS,MB A7191</td></tr><tr><td colspan="4"></td><td colspan="2">Document Number</td><td colspan="2">PGRAA LA-7191P M/B</td></tr><tr><td colspan="4"></td><td colspan="2">Date:</td><td colspan="2">Friday, September 16, 2011</td></tr><tr><td colspan="4"></td><td colspan="2">Sheet</td><td colspan="2">45 of 50</td></tr></table>					Security Classification		Compal Secret Data		Compal Electronics, Inc.		Issued Date		2010/09/09		Deciphered Date		2011/09/09		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		SCHEMATICS,MB A7191						Document Number		PGRAA LA-7191P M/B						Date:		Friday, September 16, 2011						Sheet		45 of 50	
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PIR (Product Improve Record)

PGRAA LA-7191P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.0 TO 0.1

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
09/13	04		Change RC11 from 22 ohm to 0 ohm	For SDXC SDA application
09/13	29		Change R347 to @ and R564 to mount	For LVDS dual channel select
09/21	8		Change C890,C891,C894 from 470u to 330u.	For cost reduction
09/21	8		Change C10,C11,C12 330u from D2 to OSCON.	For cost reduction
09/24	33		Remove R380,R382	For ENE has fixed entry test mode issue.
09/25	35		Add H24	For J3g mini card stand off
09/25	13		Change JP1 to JMKM, JHDD to JHDD1, JODD to JODDB	For MKM,HDD,ODD/B Conn.
09/26	27		Del Felica schematic	For meet PRD
09/26	32		Add Subwoofer schematic	For meet PRD
09/26	31		Del Rall,CA58,CA59,CA60,JA1	For reduce audio schematic
09/26	32		Change UA8 subwoofer amplifier pin6 contact from +5VS to +5VALW	For audio sleep & music
09/26	11,12,26,28,30,32		Update JDDR1,JDDRH,USB,JHDD1,JHDD2,JODDB,JLAN,JUSB30,JSUB connector	For connector list
09/26	28		Del UL3,RL4,RL23,LL1,LL3,CL9,CL13,CL28,CL29	For 1G LAN only
09/26	28		Change ULL1,RL23 BOM structure from 8105ELD0@ to 8105E@	For LAN schematic update
09/26	26		Add JHDD2,C363-C366,C371-C374	For LAN schematic update
09/26	32		Add BT schematic	For dedicated BT
09/26	35		Delete SW1 and SW4 and update JTPL pin define	For move to small board
09/26	35		Update JTPL pin define	For small board update
09/26	32		Combine FP and JTPL schematic	For small board update
10/12	05		Change Fan Control Circuit	For PWM FAN
10/12	06		Change PCIE AC capacitor from 0.22uF to 0.1uF	For nVIDIA request
10/12	09		Change R122,R252 from 100 ohm to 1K_0402_5% ohm	For Intel Design Guide V1.5 request
10/12	13,14		Remove LVDS Signal from VGA Board, RV125	DIS only support EDP
10/12	14		Mirror JLVDS pin define	For Layout Routing
10/12	14		Change R112 from 100K ohm to 10K ohm	
10/12	18		Remove R347, Change R228 form 10K ohm to 1K ohm	Only support Dual Channel, follow Intel design guide
10/12	22		Remove R444	Only support MAXIM145668
10/12	23		Remove L22,C509 change to test point T30	On-die VR default support
10/12	23		Remove R483,C280 change to test point T36	On-die VR default support
10/12	24		Remove R498 change to test point T41	On-die VR default support
10/12	24		Remove L20,C302 change to test point T42	On-die VR default support
10/12	24		Remove L17,C296 change to test point T43	On-die VR default support
10/12	26		Reverse JP10 pin define	Follow FFC Pin define
10/12	26		Remove SWS	Cancel function test
10/12	26		Direction connection SLP_CHG_M3, SLP_CHG_M4, Remove R1445	Only support MAXIM145668
10/12	28		Remove LL5, add CL35	For EMI request
10/12	29		Change RC17 from 0 ohm to 22 ohm	For xD issue
10/12	31		Remove RA34	Support Sleep & Music function
10/12	32		Remove R361	Pull Up 10K ohm at PCH side
10/12	33		Remove R380,R382	Don't avoid to EC entry ENE test mode
10/12,14	33,34		Change L1D +3VALW to +3VL	
10/12	22,35		Change Q32,Q51 (single) to Q209 (dual)	For cost reduction
10/13	35		Change R22 from 63.4 ohm to 90.9 ohm	For Power Board LED request
10/13	34		ADD R393,C457	For EMI request
10/14	13		Remove RV18, Direct connection to MKM connector	PCH Side already have option item
10/14	26		Update JHDD2 Connector	For connector list
10/14	16,20		Remove HDMI signal from PCH side	For support Optimus Huron River 2.0
10/14	22,33		Add CIR BTO@	Reserve to CIR
10/15	13		Add R566	Fine tune vga_clk sequence
10/18	5,10		Remove XDP connector & other component	For layout routing request
10/18	30		Change USB3.0 IC from SA000048H10(ES/CS sample) to SA000048H00(QS Sample)	
10/18	33		Change R172 to @	Due to the pull high resister will be in Cap sensor board
10/18	34		Reserve power rail +3VL for Hall sensor	

PIR (Product Improve Record)
PGRAA LA-7191P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION	LIST	PURPOSE
10/22	26		Q6 change to always mount		
10/22	33,36		Change Q6(single) & Q41(single) to Q6(Dual)		For cost reduction
10/25	20		Change R223 & R229 BOM Structure to OPTw		For Optimus
10/25	13		Change C15 & C16 P/N: SE00000QKNO		B+
10/27	18		Add clear Pass-word function in PASSWORD_CLEAR# (PCH_GPIO56)		By Customer demand
10/27	22		Change PCH_GPIO37 pull down R547 value from 100k ohm to 10k ohm		By Intel Check list V1.5 demand.
10/28	33		Change EC GPXIOD04 from SLP_CHG# to OTP_HW		By PWR demand.
10/28	33		Add D26, R359 for OPT_HW function.Remove R1428, R439 for SLP_CHG#.		By PWR demand.
11/1	23		Add net +VCCAFDI_VRM to U2.AP16		
11/4	34		Change LID SW power rail to +3VL		
11/4	15		Add test point at JCRT pin4, pin11		By CIC demand
11/5	17~25		Change PCH P/N from SA00003P440 to SA00004EE50		By SMT demand
11/5	27		Remove D24 and add Q39 to avoid SUSP# leakage		Avoid SUSP# leakage
11/5	27		Add level shift circuit for WL_OFF#		Avoid leakage from WLAN to PCH.
11/8			Change P/N from SCH751H010 to SCS00002G00		For cost reduction
11/9	23		Change R480 from SD002000080 to SD013000080		For layout placement
11/9	24		Change C326 from SE042104K80 to SE076104K80		For layout placement
11/9	23		Change R477 from SD002000080 to SD013000080		For layout placement
11/9	27		Change CM9 from SE053475280 to SE107475K80		For layout placement
11/10	23		Add R583		For CRT noise issue
11/10	32		Change Sub-woofer from AGND to DGND		For Sub-woofer issue
11/12	18		Add R584		For Panel select
11/16	33		Chagne D26 from always mount to @		Reserve to Power team use
11/16	35		Chagne H21 footprint from 4P7 to 4P2x4P7, H22 footprint from 4P7 to 4P7x5P6		ME drawing
11/17	27		Change Q36(single) & Q39(single) to Q210(Dual)		For cost reduction
11/17	26		Change JUSB footprint from SP060004B00 to DC233007P00		For ME request
11/17	35		Reverse JLED Pin define		For SB layout request
11/18	35		Add Screw Hole H24 & H25		For ME request
11/18	35		Change JLED Connector		For ME request
11/18	28		Add R392,R403,R419,R429,R430,R431,R439,R434		For EMI ISN rsi request
11/18	14		Add D15 for ESD		Reserve for DVT test
11/18	23		Change R583 from 0 ohm to 1 ohm		For PCH CRT wave line issue
11/22	5		Change D86 P/N from SC100000Y10 to SC100001M00		For PUR suggest
11/22	34		Change UG1 P/N from SA000039900 to SA00004GB00		By IC revision update
11/25	35		Change H22 footprint from H_4P7x5P6 to H_4P2x4P7		For ME drawing
11/25	32		Change CA72 form 2.2uF to 4.7uF		For Sub-woofer noise issue
11/25	34		Remove H24,H25		For layout request
11/26	14		Add D15,D17,R337		For EC (Panel) Back light & PWM issue
11/29	10		Add NET NAME at T22,T23,T24,T25,T28 Delete T-PAD at T6、T5、T25、T28、T27、T24、T23、T22、T21、T19、T18、T12、T11		For layout request
11/30	35		Change R404,R819 power plane from +5VS to +3VS		For LED issue
11/30	24		Add C1207,C1208		For cost reduction
11/30	28		Change CL37 to 180PF and change BOM to reserved CL38 Change BOM to mounted DL1 and DL2 Change BOM to mounted CL683 and CL684		For EMI request
12/1	35		Change R22 from 90.9 ohm to 150 ohm		For LED

PIR (Product Improve Record)

PGRAA LA-7191P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
12/9	31,32		Add Sleep & Music circuit	Modify sleep & music function
12/9	30		Change +1.5V to +1.05V Transfer power plane from +5VALW to +3V	Avoid leakage current
12/9	33		Change U44 & C818 to unmount, mount R446	For cost reduction
12/13	18		Change R584 BOM structure from EDP@ to DIS@	For BOM Structure error
12/13	30		Mount LT1,LT2,LT4	For EMI request
12/13	17		Change U13 P/N from SA00003IN00 to SA00003K800	For support Dual and quad SPI.
12/14	31		Add Net Name & Sleep-Music Schematic	For Subwoofer Sleep-Music funtion
12/14	31		Add MONO_IN change page symbol	For Moving Beep noise Schematic to page 32
12/14	32		Add Beep noise schemtic & MONO_IN change page symbol	For Moving Beep noise Schematic to page 32
12/15	31		Change Net Name & Sleep-Music Schematic	For Subwoofer Sleep-Music funtion
12/17	31		Modify Net Name & Sleep-Music Schematic & symbol	For Subwoofer Sleep-Music funtion
12/20	14		LED_PWM add R126 10K ohm to GND	For Samsung panel can not adjust system backlight issue
12/20	14		Change R103 & R332 footprint from 0402 to 0603	For DXP layout co-lay issue
12/21	26		Change JHDD2 P/N to SP010015H00	For SMT assembly issue
12/23	9,36		Need mount PV30, Unmount +1.5V to +1.5VS part	For cost down plan
12/23	19		un mount U12,C250 and mount R259 for cost down purpose	For cost down plan
12/23	34		Unmount C836 for cost down purpose.	For cost down plan
12/23	9		Unmount C877 for cost down purpose.	For cost down plan
12/23	15,16		Change P1 & P2 form 1.1A to 0.5A part	For cost down plan
12/23	33		Un-mount R359	EC do not support this function
12/23	34		Change UG1 from TSH35TR to TSH352TR	For customer request
12/27	9		Change R74 & R75 from 100 ohm to 10 ohm	For Intel Checklist V1.5 updated.
12/27	8		Change C12 P/N from SF000002Z00 to SGA20331E10	For cost down plan
12/30	11		Unmount C218	For cost down plan
12/30	33,34		Add KB9012 can co-lay KB930 circuit use BOM Structure to control different component for different EC	For cost down plan
12/31	14		Change R126 from 10K to 47K	Prevent EC pin damage cause MB NG
12/31	9		change CPU GFX Core bulk cap C873 from 330uF to 560uF	To prevent Huron-River CPU_CORE PWM IC abnormal shutdown issue
12/31	31		change Net-name from sleep & music switch	To prevent S3 subwoofer i-pod noise
12/31	32		Add RA51 & CA73 for S3 subwoofer sleep & music	To prevent S3 subwoofer i-pod noise
1/3	21		Add C473	For ESD request
1/4	34		Remove UG4	For customer request
1/5	35		Add H27	For ME request
1/5	24		Unmount C333 & C515, Change L19 & L21 from inductotr to bead	For cost down plan
1/10	26		Unmount C426	For cost down plan
1/10	26		Unmount R399, always mount R544	PCBA with dGPU device lose issue now
1/12	8,9		Change C10,C11,C875 from 330uF to 390uF	For BOM change
1/13	26		Remove C426	For cost down plan
1/13	26		Remove C363, C372, C373, C374	S/B have part and layout limitation
1/13	26		Remove C352, C353, C354, C355, C360	S/B have part and layout limitation
1/17	21,30		Mount C473,DT2	For ESD request
1/18	19		Mount U12,C250, Unmount R259	Need double confirim this cost down plan
1/18	28		Change LAN chip form 8111E-VB to 8111E-VL	For cost down plan
1/19	32		Change RA51 from 20.5K to 12K	For Subwoofer noise issue
1/19	14		Change R103 & R332 footprint from 0603 to 0402	For DFX request

PIR (Product Improve Record)

PGRAA LA-7191P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.3 TO 0.4

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1/20	8		Change C2 from 330uF to 470uF & C7,C9 from 470uF to 330uF	For Power request
2/8	27,35		Change Wimax8 to always mount	For Customer request
2/18	8,9		Remove C391, C351, C350, C349, C215, C214, C221, C223, C209, C131 C126, C220, C219, C222, C891, C894	For Power layout request
2/25	34		Add R993 and R994 for keyboard backlight +3VS and +5VS option	For Customer request
3/2	31,32		Modify Audio and subwoofer writing descritption	For avoiding confusion
3/3	13,16		Swap HDMI port 0 and port 2 from MXM conn.	To meet MXM spec.
3/3	09		Change C875 from SF000002000 to SF000002200.	For ME request to avoide ME impact
3/8	13		Un-mount D25	For 3D mark performance low issue on battery mode
3/9	24		Remove C333 and C515	For ME JTPL changing to non-ZIF connector will has ME impact
3/10	26		Add 1pcs C1211 680pF 0603 on +5VALW and close to R148 Add 2pcs C1209,C1210 680pF 0603 on +5VL and close to R149	For EMI request that USB/B will couple with Audio traces (165MHz) through FFC cable
3/10	35		Change JTPL from SP01000ZL00 to SP01000YG00	For ME request
3/10	31		Delete RA36, RA39, RA35, RA38, RA30, RA37 Add CA38, RA888, RA889, CA13, RA40, RA891, RA890, CA39	Add AC reference voltage circuit for UA2
3/10	32		Change CA72 package from 0805 to 0603 and add CA74 0402	For tuning subwoofer on-off time
3/10	31		Change CA21, CA22, CA38 and CA39 to 4.7uF 0603	For audio issue
3/10	34		Change R394 from 33ohm to 100ohm, C454 from 33pF to 100pF	For EMI request
3/14	17		Change BOM structure of R397 and C86 from un-mount to mount	For EMI request about ISN and SPI issue
	28		Change CL37 to reserve	
3/14	32		Change CA70 and CA73 from 2.2uF to 0.47uF	For popo issue
3/15	35		Add PCH HM65 B3 PN	

PIR (Product Improve Record)
PGRAA LA-7191P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.4 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
4/2	17		Modify clear CMOS jumper's name from JCOMS to JCMOS	For jumper naming rule
	34		Modify R993 BOM structure from KBL@ to @ and R994 from @ to KBL@	For customer request
	32		Change inductors LA4, LA5 (SHI00002T00) to 0ohm RA7,RA8 (SD013000080)	For subwoofer current
	17		Un-mount R363, R330, R278 and R306, R295, R301	For S5 power saving
	31		Add CA40, CA41 and un-mount CA21, CA22	For Audio THD+N fail issue
	16		Change HDMI choke L8, L9, L10 and L11 from SM070001310 to SM070001U00	For HDMI eye diagram fail
	14		Change D84 PN from SCA00000U10 to SC600001600	For source common
	35		Change PCB PN to DA20IB00100	For MP use
4/11	31		Change CA21 & CA22 package from 0603 to 0402	For layout request
	14		Reserve a AND gate to pull BK_OFF# timing in for eDP panel	For Samsung 3D panel white line issue
	31		Add 0.1U CA51 to cross on GND and AGND	For layout request
4/19	14		Change R103 to 0ohm and BOM structure is DIS@	For Samsung 3D panel white line issue
			Change D15 BOM structure to OPT@	
	13		Change PR628 to 150K ohm	For tuning OPT VGA_CORE sequence
4/26	31		Change RA889 and RA891 from 10K to 8.2K	For audio performance tuning

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